Pragati Engineering College
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A Report on

Online Guest Lecture

On

"Low Power VLSI Design"

on 10th September 2025

Organized by

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Under

ECE Student Association

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Organizes

Online Guest Lecture on

"Low power VLSI Design"

by

Dr Sriadibhatla Sridevi, Professor &HoD ,
Department of VLSI,
School of Electronics Engineering, VIT , Vellore

Date :10-09-2025

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(Autonomous)

Learning is Supreme Deity

PRAGATI ENGINEERING COLLEGE

(Approved by AICTE, Permanently Affiliated to JNTUK Kakinada & Accredited by NBA)
ADB Road, Surampalem – 533 437, Near Peddapuram, E.G.Dist., A.P.
Ph: (08852) – 252233, 252234, 252235 Fax: (08852) – 252232

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

DATE: 12.09.2025

A Report on

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on

«Low Power VLSI Design»

On 10th September 2025, a Guest Lecture on "Low Power VLSI Design" was organized by the Department of ECE for the second-year B.Tech ECE students under the ECE Student Association. The session was conducted in Conference Hall at Main Block and EG-6 Computer Lab-1. The lecture was delivered by Dr. Sriadibhatla Sridevi, Professor & HOD, Department of VLSI, School of Electronics Engineering, VIT University, Vellore, who served as the resource person. The event was coordinated by Mrs. L. Gaviramma, Assistant Professor, Mr. T. Sekhar, Assistant Professor, and Mr. M Ravi Kumar, Assistant Professor, Department of ECE.

Total 90 Students were Participated in this Guest Lecture from III Year

About the Resource Person:

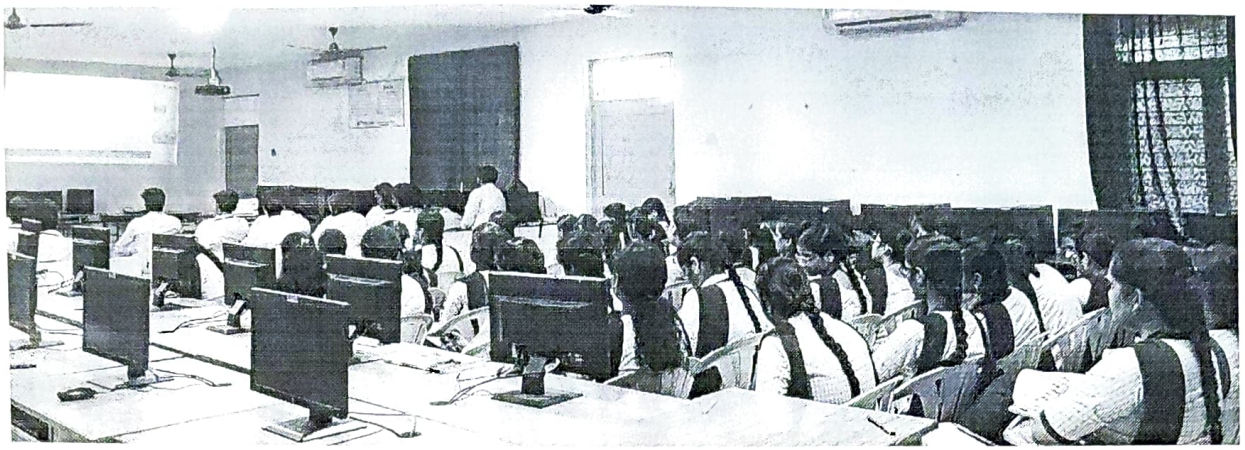
SRIADIBHATLA SRIDEVI received the B.Tech. degree in Electronics and Communication Engineering and the M.Tech. degree in Communication Engineering from Jawaharlal Nehru Technological University, Hyderabad, India, and the Ph.D. degree in VLSI design from Andhra University, Visakhapatnam, India.

Since August 2013, she has been with the School of Electronics Engineering, Vellore Institute of Technology (VIT), Vellore, India, where she is currently a Professor and HOD, Department of VLSI. She has 25 years of teaching experience. Five scholars have completed Ph.D. studies successfully under her guidance and also guiding four Ph.D. scholars.

She has published 59 papers in international journals and conferences.

Her current research interests include Hardware implementation of machine learning algorithms, low power memory design and low power digital design. She is a Senior member IEEE and Life Member of the Instrument Society of India (ISOI).

Photo of Inviting the guests (Dr. G Naresh, Prof. and Principal, Recourse Person
Attended online Dr. Sriadibhatla Sridevi and Dr. V Prasanth, Assoc. Prof. and HOD-ECE with students in conference Hall



Students attended in EG-6 Computer Lab

Dr. G. Naresh, Professor and Principal, given the speech,"It gives me immense pleasure to inaugurate today's Guest Lecture on *'Low Power VLSI Design.'* VLSI has become one of the most significant areas in modern electronics, especially in the context of designing energy-efficient systems for portable and high-performance applications. Low power design is no longer an option—it is a necessity for sustainable technology. I am glad that our Department of ECE has taken this initiative to expose students to this crucial domain through an expert lecture. I warmly welcome our distinguished resource person, **Dr. Sriadibhatla Sridevi, Professor and Head, Department of VLSI, School of Electronics Engineering, VIT University, Vellore**, and thank her for joining us today to share her vast expertise. I encourage all students to make the best use of this session to strengthen both their academic knowledge and research outlook."

Introduction

Power has now become a primary design constraint in modern VLSI systems, alongside performance. Very-Large-Scale Integration (VLSI) allows millions or even billions of transistors to be placed on a single chip. With the scaling of CMOS technology, power consumption has emerged as a major bottleneck. Applications such as mobile devices, wearables, IoT systems, and data centers demand low-power designs to ensure efficiency and reliability.

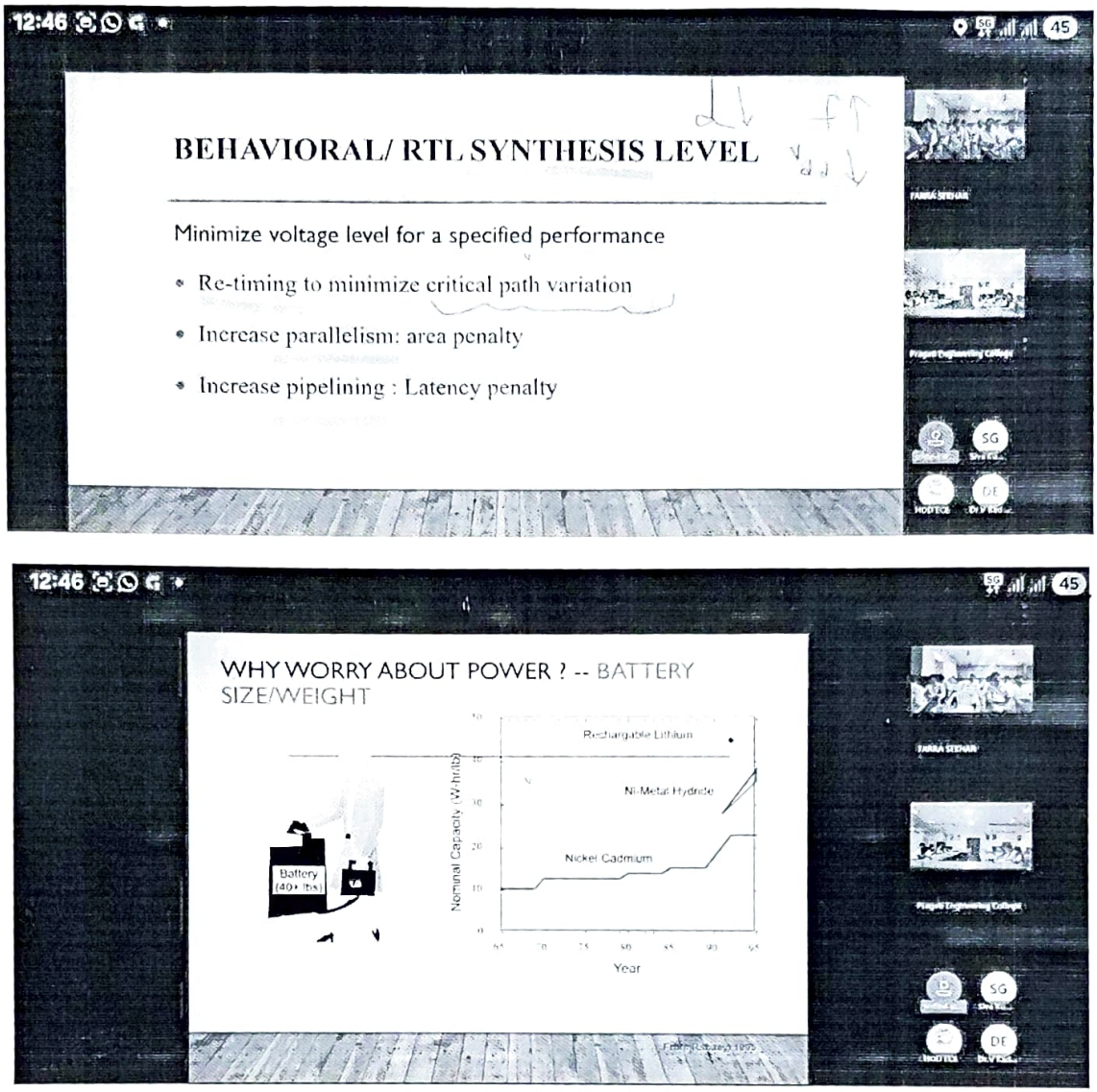
Objectives of the Guest Lecture

1. To provide an introduction to the importance of power as a key design constraint in modern VLSI systems.
2. To explain the sources of power dissipation in CMOS circuits and their impact on circuit performance.
3. To familiarize students with various low power design techniques at the technology, circuit, logic, architectural, and system levels.
4. To demonstrate real-world applications and case studies such as ARM processors and smartphone SoCs in the context of low power design.
5. To create awareness about industry-standard CAD tools and methodologies used for low power VLSI design.
6. To highlight future research trends and opportunities in the area of energy-efficient electronics.

Session Highlights:

Motivation for Low Power Design

The need for low power design arises mainly from the limitations of battery life in portable devices, the high cost of heat dissipation and cooling, and the reliability issues caused by excessive temperature. Energy-efficient computing has also become essential to achieve sustainability in large-scale computing. For example, a smartphone SoC is expected to deliver high performance while operating within a power budget of less than 5 watts.



Screen Shot of the session

Sources of Power Dissipation in CMOS Circuits

Power consumption in CMOS circuits can be divided into three categories. Dynamic power, also called switching power, occurs due to charging and discharging of capacitance during logic transitions and is directly influenced by switching activity, load capacitance, supply voltage, and clock frequency. Short-circuit power arises during switching when both PMOS and NMOS transistors briefly conduct simultaneously. Static power, or leakage power, results from subthreshold leakage, gate oxide leakage, and junction leakage, which become significant in advanced technologies below 65 nm.

Techniques for Low Power VLSI Design

Low power design can be achieved at multiple levels. At the technology level, methods such as high-k dielectrics, FinFETs, SOI technology, and multi-threshold voltage processes are used. At the circuit level, techniques like voltage scaling, optimal transistor sizing, stacking, and efficient logic styles help reduce power. At the logic level, approaches such as logic restructuring, clock gating, and operand isolation are widely used. Architectural-level methods include pipelining, parallelism, DVFS (Dynamic Voltage and Frequency Scaling), and power gating.

Case Studies and Applications

Practical examples of low power design include the ARM Cortex-M0 processor, which is optimized for ultra-low-power IoT applications. It supports sleep modes, clock gating, and a reduced instruction set to minimize power consumption. Similarly, smartphone SoCs adopt multiple power domains and integrate techniques such as DVFS, power gating, and clock gating to balance high performance with energy efficiency.

6. CAD Tools for Low Power Design

- Synopsys Design Compiler – Low-power synthesis.
- Cadence Voltus – Power integrity and analysis.
- Mentor Graphics (Siemens) – Power-aware verification.
- Standards: UPF (Unified Power Format), CPF (Common Power Format).

7. Future Trends

- Near-threshold and sub-threshold computing.
- Emerging devices: Tunnel-FETs, Spintronics, NEMS.
- AI/ML-based power estimation methods.
- 3D ICs and advanced packaging techniques.

Learning Outcomes of the Guest Lecture

1. Students gained an understanding of why power has become a critical design constraint in modern VLSI systems.
2. They learned about the different sources of power dissipation in CMOS circuits, including dynamic, short-circuit, and leakage power.
3. They became familiar with low power design techniques applied at multiple levels — technology, circuit, logic, architectural, and system.
4. They explored real-world applications through case studies such as ARM Cortex-M0 processors and smartphone SoCs.
5. The session motivated students to apply low power concepts in their academic projects and future professional careers.

In his concluding remarks, Dr. V. Prasanth highlighted the importance of low power VLSI design in today's technology-driven world. He appreciated the resource person for sharing valuable insights and encouraged students to apply these concepts in their learning and future projects. He also emphasized that such expert sessions bridge the gap between academic knowledge and industry practices.

Screen Shots of concluding remarks by Dr. V. Prasanth

On behalf of the Department of ECE, we sincerely thank our esteemed resource person, Dr. Sriadibhatla Sridevi, for her insightful session. We also extend our gratitude to our Principal, faculty members, and coordinators for their support, and to all the students for their enthusiastic participation in making this guest lecture a success.

Coordinator

HOD-ECE

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