M.Tech – VLSI SD

R24

Academic Regulations
Course Structure
&
Syllabus

PRAGATI ENGINEERING COLLEGE
(An Autonomous Institution)
ADB Road, Surampalem, Kakinada District, A.P.-533 437
(Approved by AICTE, New Delhi & Permanently Affiliated to JNTUK, Kakinada)
(Recognized by UGC under sections 2 (f) and 12 (b) of UGC act, 1956)

M.Tech

(Effective for the students admitted from the Academic Year **2024-25** onwards)

ACADEMIC REGULATIONS R24 FOR M. Tech (REGULAR) DEGREE COURSE

Applicable for the students of M. Tech (Regular) Course from the Academic Year 2024-25 onwards. The M. Tech Degree of Pragati Engineering College(Autonomous) shall be conferred on candidates who are admitted to the program and who fulfill all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the State Government and Affiliating University and College from time to time.

2.0 *AWARD OF M. Tech DEGREE*

2.1 A student shall be declared eligible for the award of the M. Tech Degree, if he pursues a course of study in not less than two and not more than four academic years.

2.2 The student shall register for all 68 credits and secure all the 68 credits.

2.3 The minimum instruction days in each semester are 90.

3.0 A. PROGRAMMES OF STUDY

The following specializations are offered by various departments for the M. Tech Programme of study.

1. **M.Tech- Power Electronics and Electrical Drives**
2. **M.Tech- CAD/CAM**
3. **M.Tech- VLSI System Design**
4. **M.Tech- Computer Science and Engineering**

and any other course as approved by AICTE/ University from time to time.

3.0 B. Departments offering M. Tech Programmes with specializations are noted below:

EEE	**M.Tech- Power Electronics and Electrical Drives**
ME	**M.Tech- CAD/CAM**
ECE	**M.Tech- VLSI System Design**
CSE	**M.Tech- Computer Science and Engineering**

4.0 ATTENDANCE

4.1 **A student shall be eligible to write End Semester Examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.**

4.2 **Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the Committee.**

4.3 **Shortage of Attendance below 65% in aggregate shall not be condoned.**

4.4 **Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of that class.**

4.5 **A prescribed fee shall be payable towards condonation of shortage of attendance.**

4.6 **A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.**

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals on the basis of Internal Evaluation and End Semester Examination.

5.1 For the **theory subjects** 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the **average** of the marks secured in the two Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each mid term examination shall be conducted for a total duration of 120 minutes with 4 questions (without choice) each question for 10 marks. Semester End Exam Paper contains FIVE mandatory questions (one question from one unit) with internal choice, each carrying 12 marks for a total of 60 marks.

5.2 For **Practical subjects**, 60 marks shall be awarded based on the performance in the End Semester Examinations and 40 marks shall be awarded as internal marks, based on the day to day work-10 marks, Record-10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with a breakup marks of Procedure-15, Experimentation-25, Results-10 , Viva-voce-10.

5.3 For **Technical seminar**, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For Technical seminar, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. Out of 100 marks, supervisor awards 40% marks and remaining 60% marks are awarded by the project review committee.

5.4 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.5 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.4) he has to reappear for the End semester Examination in that subject. A candidate shall be given a chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled. For re-registration the candidates have to apply to the college by paying the requisite fees before the start of the semester in which re-registration is required.

5.6 In case the candidate secures less than the required attendance in any re registered subject (s), he shall not be permitted to write the End Examination in that subject. He shall again re-register the subject when next offered

5.7 Laboratory examination for M. Tech. programmes must be conducted with two Examiners, one of them being the Laboratory Class Teacher or teacher from the same department and the second examiner shall be appointed by the Principal from the panel of examiners submitted by the respective HoD.

5.8 Student is allowed to register for 12 week SWAYAM / NPTEL MOOC courses (recommended by BoS Chairman) and obtain required credits during II Semester itself. In any case, if a student fails in obtaining credits, he is allowed to repeat the initially opted course / change to another MOOC course or regular course and will be considered as regular candidate only. After successful completion, by the end of III Semester, he needs to submit the course certificate (through HoD) to the exam section to perform credit transfer.

5.9 In addition to credit courses, for completing the programme and obtaining degree, a student needs to complete audit courses. Audit courses will be conducted, evaluated as normal credit courses, and the assessment will be graded as Pass or Fail.

5.10 Students shall undergo mandatory summer **internship** (2 credits) for a minimum of eight weeks duration at the end of II semester of the Programme/Summer Break. A student will be required to submit a summer internship report to the concerned department and appear for an oral presentation before the committee. The Committee comprises of Head of the Department and two faculty. The report and the oral presentation shall carry 40% and 60% weightages respectively. For internship, there will be only internal evaluation of 100 marks in the III semester. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.0 EVALUATION OF PROJECT WORK(part-1 and Part-2)

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

6.1 For Project evaluation, out of 200 marks, 80 marks shall be for Internal Evaluation(40 internal marks for Project work Part-I and remaining 40 internal marks for project work Part-II) and 120 marks for the End Examination (Viva–Voce).

6.2 Student has to secure 40% of marks in the Viva–Voce examination and a minimum aggregate of 50% of total marks in Viva–Voce examination and Internal Evaluation taken together.

6.3 A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members.

6.4 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

6.5 After satisfying 6.4, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval. The student can initiate the Project work, only after obtaining the approval from the Project Review Committee (PRC).

6.6 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Project Review Committee (PRC). However, the Project Review Committee (PRC) shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.7 A candidate shall submit his status report in two stages at least with a gap of 3 months between them.

6.8 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical subjects before submission of the Thesis.

6.9 The candidate may be allowed to submit the project report, if the project work is published or accepted in a reputed national or international journal or conference.

6.10 Three copies of the Project Thesis certified by the supervisor shall be submitted to the department along with plagiarism report (<40%).

6.11 The thesis shall be adjudicated by one examiner selected by the Principal. For this, the Head of the Department shall submit a panel of five examiners, eminent in that field, with the help of the guide concerned and other PRC Members.

6.12 If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is still unfavorable, the thesis shall be summarily rejected. The candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the Principal.

6.13 The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination.

6.14 If the candidate failed in the Viva-Voce examination, the candidate shall retake the Viva-Voce examination only after three months. If he failed again the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the Principal.

7.0 Cumulative Grade Point Average (CGPA)

Marks Range (Max – 100)	Letter Grade	Level (G)	Grade Point
≥ 90	S	Excellent (S)	10
≥80 to <90	A	Very Good (A)	9
≥70 to <80	B	Good (B)	8
≥60 to <70	C	Fair (C)	7
≥50 to <60	D	Satisfactory (D)	6
<50	F	Fail (F)	0
		Absent	0

Computation of SGPA

The following procedure is to be adopted to compute the Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

The SGPA **is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e**

$$SGPA\ (Si) = \sum (Ci\ X\ Gi) / \sum Ci$$

Where Ci is the number of credits of the i^{th} course and Gi is the grade point scored by the student in the i^{th} course.

Computation of CGPA

The CGPA **is also calculated in the same manner taking into account all the courses undergone by a student over all the semester of a programme, i.e.**

$$CGPA = \sum (Ci\ X\ Si) / \sum Ci$$

Where Si is the SGPA of the i^{th} semester and Ci is the total number of credits in that semester. The SGPA and CGPA shall be rounded off to TWO decimal points and reported in the transcripts.

8.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	**CGPA to be secured**	
First Class with Distinction	≥ 7.75 without backlog history	**From the CGPA secured from 68 Credits.**
First Class	≥ 6.75	
Second Class	≥ 5.75 to < 6.75	

9.0 WITHHOLDING OF RESULTS

If the student has not paid the dues, if any, or if any case of indiscipline is pending against him, the result of the student will be withheld. His degree will be withheld in such cases.

10.0 TRANSITORY REGULATIONS

Discontinued or detained candidates are eligible for re-admission into same or equivalent subjects at a time as and when offered.

11.1 GENERAL

11.2 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

11.3 The academic regulation should be read as a whole for the purpose of any interpretation.

11.4 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

11.5 The College may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the College.

PRAGATI ENGINEERING COLLEGE: SURAMPALEM

R24

(Autonomous)

DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

R24M.TECHVLSI SYSTEM DESIGNCOURSESTRUCTURE

ISemester

S.No	Category	Subject Code	Course Title	L	P	C
1	Program Core	24041T01	CMOS Analog IC Design	3	0	3
2	Program Core	24041T02	CMOS Digital IC Design	3	0	3
4	**PROGRAM ELECTIVE-I**			3	0	3
	Program Elective	24041T03	Digital System Design			
	Program Elective	24041T04	Advanced MOSFET Modeling			
	Program Elective	24041T05	Optimization Techniques in VLSI Design			
5	**PROGRAM ELECTIVE –II**			3	0	3
	Program Elective	24041T06	CPLD and FPGA Architectures and Applications			
	Program Elective	24041T07	Advanced Computer Architecture			
	Program Elective	24041T08	Hardware Software Co-Design			
6	Credit Course	24RM1T01	Research Methodology and IPR	2	0	2
7	Program Core	24041L01	Digital System Design Laboratory	0	4	2
8	Program Core	24041L02	VLSI Laboratory-I	0	4	2
9	Audit Course	24041A01	Audit Course-1*	2	0	0
			Total Credits			**18**

***Student has to choose any one audit course listed at the end of the course structure.**

II Semester

S.No	Category	Subject Code	Course Title	L	P	C
1	Program Core	24042T08	Low Power VLSI Design	3	0	3
2	Program Core	24042T09	Embedded System Design	3	0	3
4	**PROGRAM ELECTIVE-III**			3	0	3
	Program Elective	24042T10	Soft Computing Techniques			
	Program Elective	24042T11	DSP Processors & Architecture			
	Program Elective	24042T12	CAD for VLSI			
5	**PROGRAM ELECTIVE –IV**			3	0	3
	Program Elective	24042T13	System on Chip Design			
	Program Elective	24042T14	CMOS Mixed signal Design			
	Program Elective	24042T15	ASIC Design			
6	Program Core	24042L03	Embedded System Design Laboratory	0	4	2
7	Program Core	24042L04	VLSI Laboratory-II	0	4	2
8	Mini Project	24042S01	Technical Seminar	2	0	2
9	Audit Course	24042A02	Audit Course-2*	2	0	0
			TotalCredits			**18**

***Student has to choose any one audit course listed at the end of the course structure.**

- Eight weeks Mandatory Industrial Training/Internship during summer / semester break

IIISemester

S.No	Category	SubjectCode	Course Title	L	P	C
1	**PROGRAM ELECTIVE-V**			3	0	3
	MOOCS	24043M01	MOOCS (NPTEL)-12 Week Course Recommended By The Department Relevant To The Program. **(OR)**			
	Program Elective	24043T17 24043T18 24043T19	• Test and Testability • Semiconductor Memory Design and Testing • VLSI Signal Processing			
2	**OPEN ELECTIVE**			3	0	3
	MOOCS	24043M02	MOOCS (NPTEL)-12 Week Course Recommended By The Department Relevant To The Program. **(OR)**			
	Open Elective		Courses offered by other departments in the college • Nano Technology • Principles of Cyber Security • Fundamentals of Electric Vehicles			
3	Internship	24043I01	**Internship** (Performed during Summer after first year)	0	0	2
4	Project	24043P01	**Project Work Part-I**	0	20	8
			Total Credits			**16**

Students going for Industrial Project/Thesis will complete these courses through MOOCs.

IVSemester

S.No	Category	SubjectCode	Course Title	L	P	C
1	Project	24044P02	**Project Work Part-II**	0	32	16
			Total Credits			16

NOTE:

- ***Audit Course 1 :**
  1) Writing Skills for Research Paper
  2) Sanskrit for Technical Knowledge
- ***Audit Course 2 :**
  1) Pedagogy Studies
  2) Personally Development through Life Enlightenment Skills.

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DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS

M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

CMOS ANALOG IC DESIGN

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Understand the basic parameters of MOS transistor and different models	K3
CO2	Understand the basic theory of MOS transistors and Different characteristics'	K2
CO3	Study the Different application of C-MOS transistor	K3
CO4	Design the Op-Amps and its application using C-MOS transistor	K3
CO5	Learn the basics theory of open loop comparators.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3	2	2	1	0	0	0	0	0	0	0
CO2	2	3	2	2	2	0	0	0	0	0	0	0
CO3	3	2	3	2	2	0	0	0	0	0	0	0
CO4	2	2	2	2	1	0	0	0	0	0	0	0
CO5	3	2	2	2	2	0	0	1	0	0	0	0

COURSE CONTENT

UNIT I

MOS Devices and Modeling The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT II

Analog CMOS Sub-Circuits MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT III

CMOS Amplifiers Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT IV

CMOS Operational Amplifiers Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAMP.

UNIT V

Comparators Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete- Time Comparators.

TEXT BOOKS	
1.	CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010
2.	Analysis and Design of Analog Integrated Circuits- Paul R. Gray, PaulJ. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.
REFERENCE BOOKS	
1.	Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2.	Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
3.	CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI
WEB RESOURCES	

PRAGATI ENGINEERING COLLEGE: SURAMPALEM

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DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS

M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

CMOS DIGITAL IC DESIGN

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	Basic knowledge in VLSI and Mos transistors concepts	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Remember the basic concepts of NMOS logic and inverter devices used in portable consumer devices	K3
CO2	Understand the design of transmission gated used to implement analog switches and multiplexers	K2
CO3	Apply the MOS logic and concept of flip flops for sequential circuits used temporary storage of data or delay signals	K3
CO4	Analyze dynamic logic circuits used in temporary storage of signal using various load capacitances.	K3
CO5	Compare different type of memory devices used for storage	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	2	2	1	2		1				2	1
CO2	1	1	3	1	2		1				2	2
CO3	1	2	3	2	2		1				2	1
CO4	2	2	2	1	2		1				2	2
CO5	**1**	2	3	1	1		1				2	1

COURSE CONTENT

UNIT I

MOS Design Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic**.**

UNIT II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT III

Sequential MOS Logic Circuits Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT IV

Dynamic Logic Circuits Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT V

Semiconductor Memories Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXT BOOKS	
1.	Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2.	CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.
REFERENCE BOOKS	
1.	Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2.	Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, 2nd Ed., PHI
WEB RESOURCES	

PRAGATI ENGINEERING COLLEGE: SURAMPALEM

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DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS

M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

DIGITAL SYSTEM DESIGN

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Analyse various Minimization Procedures for minimizing Switching functions and Camp Algorithms.	K4
CO2	Design PLD's & PLA by using Minimization and Folding Algorithms	K3
CO3	Design the Large-Scale Digital Systems	K3
CO4	Analyse the Fault Diagnosis in Combinational Circuits.	K4
CO5	Discuss the Fault Diagnosis in Sequential Circuits and its Experiments.	K2

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2										
CO2	3	2	2									
CO3	3	1	3									
CO4	3	3										
CO5	3	1	1									

COURSE CONTENT

UNIT I

Minimization Procedures and CAMP Algorithm: Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT II

PLA Design, Minimization and Folding Algorithms: Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT III

Design of Large Scale Digital Systems: Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT IV

Fault Diagnosis in Combinational Circuits: Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT V

Fault Diagnosis in Sequential Circuits: Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS	
1.	Logic Design Theory-N. N. Biswas, PHI,1993.
2.	Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001,TMH
3.	Digital system Design usingPLDd-Lala,2003
REFERENCE BOOKS	
1.	Fundamentals of Logic Design – Charles H. Roth, 5th Ed., CengageLearning.
2.	Digital Systems Testing and Testable Design – MironAbramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & SonsInc,2003
WEB RESOURCES	

PRAGATI ENGINEERING COLLEGE: SURAMPALEM

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DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS

M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

OPTIMIZATION TECHNIQUES IN VLSI DESIGN

Course Category	Professional Core	**Course Code**	
Course Type	Theory (Elective-IV)	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment**	40
		Semester End Examination	60
		Total Marks	100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Compare various statistical modelling methods such as Monte carlo techniques, Pelgroms methods, principle component based and quad tree based modeling methods.	K3
CO2	Analyze the systems by using concepts of high level and gate level statistical methods	K2
CO3	Analyze complete knowledge regarding the various algorithms used for optimization of power and area.	K3
CO4	Develop the real time applications using optimization techniques such as Genetic Algorithms.	K3
CO5	Apply CMOS technology -specific layout rules in the placement and routing of transistor sand to verify the functionality, timing and power	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	-	1	-	2	2	-	-	-	-	-	-	-
CO2	-	3	2	3	-	-	-	-	-	-	-	-
CO3	-	1	-	4	2	-	-	-	-	-	-	-
CO4	-	-	-	3	-	2	-	-	-	-	-	-
CO5	**1**	2	-	3	3	-	-	-	-	-		-

COURSE CONTENT

UNIT I

Statistical Modeling Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom"s model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models

UNIT II

Statistical Performance, Power and Yield Analysis Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, Highlevel statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation

UNIT III

Convex Optimization Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Polynomial fitting

UNIT IV

Genetic Algorithm Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning- automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement GASP algorithm- unified algorithm

UNIT V

FPGA Routing Procedures and Power Estimation Global routing-FPGA technology mapping-circuit generation-testgeneration in a FPGA frame work-test generation procedures, Power estimation-application of GA Standard cell placement-GA for ATG- problem encoding- fitness function-GA Vs Conventional algorithm

TEXT BOOKS	
1.	Statistical Analysis and Optimization for VLSI: Timing and Power -AshishSrivastava, Dennis Sylvester, David Blaauw, Springer, 2005
2.	Genetic Algorithm for VLSI Design, Layout and Test Automation -PinakiMazumder, E.Mrudnick, Prentice Hall,1998
REFERENCE BOOKS	
1.	Convex Optimization Stephen Boyd, Lieven Vandenberghe, Cambridge University Press,2004
WEB RESOURCES	

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SYLLABUS

M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment**	40
		Semester End Examination	60
		Total Marks	100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	understand various architectures and device technologies of PLD's	K2
CO2	discuss the architectures and applications of FPGA Programming Technologies	K2
CO3	understand various architectures and programming technologies of SRAM Programmable FPGAs	K2
CO4	Discuss various architectures and programming technologies of Anti-Fuse Programmed FPGAs	K2
CO5	design examples of various CPLD and FPGA Applications and to discuss the General Design Issues	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	1	1	0	0	0	0	0	0	0	0	0
CO2	3	2	2	2	2	0	0	0	0	0	2	0
CO3	3	2	2	2	2	0	0	0	0	0	2	0
CO4	3	2	2	2	2	0	0	0	0	0	2	0
CO5	**3**	3	3	3	3	0	0	0	0	0	3	0

COURSE CONTENT

UNIT I

Introduction to Programmable Logic Devices Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices
– Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation**.**

UNIT II

Field Programmable Gate Arrays Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT III

SRAM Programmable FPGAs Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT IV

Anti-Fuse Programmed FPGAsIntroduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures

UNIT V

Design Applications General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

TEXT BOOKS	
1.	Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition,1994.
2.	Digital Systems Design - Charles H. Roth Jr, LizyKurian John,2nd Ed., Cengage Learning,1998
REFERENCE BOOKS	
1.	Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India,1995.
2.	Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/ SamihaMourad, Pearson Low Price Edition,1994.
3.	Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier Newnes,2008.
4.	FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series,2004.
WEB RESOURCES	
1.	https://nptel.ac.in/courses/...contents/IIT%20Kharagpur/.../Pdf/Lesson-20.p...
2.	https://nptel.ac.in/courses/117108040/35
3.	https://nptel.ac.in/.../Field%20Programmable%20Gate%20Arrays%20
4.	pldworld.org/html/technote/intro.cpld.fpga.design.pdf

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SYLLABUS

M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

ADVANCED COMPUTER ARCHITECTURE

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	Basics of advanced computer architeture	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Discuss the organisation of computer-based systems and how a range of design choices are influenced by applications	K3
CO2	Understand different processor architectures and system-level design processes.	K2
CO3	Understand the components and operation of a memory hierarchy and the range of performance issues influencing its design.	K3
CO4	Understand the organisation and operation of current generation parallel computer systems, including multiprocessor and multicore systems	K3
CO5	Develop systems programming skills in the content of computer system design and organisation.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)											
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	2	2	2	2	0	0	0	2	0	0	1
CO2	2	3	2	3	2	0	0	0	1	0	0	2
CO3	2	2	2	3	2	0	0	0	1	0	0	1
CO4	2	3	2	2	3	0	0	0	1	0	0	1
CO5	**3**	2	3	2	2	0	0	1	1	0	0	1

COURSE CONTENT

UNIT I

Fundamentals of Computer Design Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl‟slaw. Instruction set principles and examples-Introduction, classifying instruction set- memory addressing- type and size of operands, Operations in the instruction set.

UNIT II

Pipelines Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT III

Instruction Level Parallelism (ILP)-The Hardware Approach Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo‟s approach, Branch prediction, High performance instruction delivery- Hardware based speculation. ILP Software Approach Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT IV

Multi Processors and Thread Level Parallelism Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT V

Inter Connection and Networks Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS	
1.	John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier,2002
REFERENCE BOOKS	
1.	John P. Shen and Miikko H. Lipasti - Modern Processor Design : Fundamentals of Super ScalarProcessors,2013
2.	Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill,1984
3.	Advanced Computer Architecture - A Design Space Approach -DezsoSima, Terence Fountain, Peter Kacsuk , PearsonEd,1997
WEB RESOURCES	
1.	http://scitechconnect.elsevier.com/category/computer-science/
2.	https://www.sztaki.hu/en/science/departments/lpds
3.	http://www.ecs.umass.edu/ece/koren/arith/
4.	https://onlinelibrary.wiley.com/doi/full/10.1002/9780470050118.ecse071

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M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

HARDWARE SOFTWARE CO-DESIGN

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	acquire the knowledge about system specification and modeling.	K2
CO2	learn the formulation of partitioning the hardware and software	K2
CO3	analyze about the hardware and software integration	K2
CO4	study the hardware design languages and its components	K2
CO5	formulate the design specification and module creation	K2

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2	1	1								
CO2	3	2	2	1								
CO3	3	3	2	1								
CO4	3	2	1	1								
CO5	3	3	3	1								

COURSE CONTENT

UNIT I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure
Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT IV

Design Specification and Verification: Design, co-design, the codesign computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT V

Languages for System – Level Specification and Design-I: System level specification, design representation for system level synthesis, system level specification languages.
Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS	
1.	Hardware / Software Co- Design Principles and Practice – JorgenStaunstrup, Wayne Wolf – 2009, Springer.
2.	Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers
REFERENCE BOOKS	
1.	A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer Publications.
2.	
WEB RESOURCES	

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SYLLABUS

M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

Digital System Design Lab

Course Category	Professional Core	**Course Code**	
Course Type	Laboratory	**L-T-P-C**	4-0-0-2
Prerequisites		**Internal Assessment**	40
		Semester End Examination	60
		Total Marks	100

COURSE OBJECTIVES: The objectives of the course are to	
1	To understand about VHDL and Verilog Programming in all available styles.
2	To understand differences between Verilog and VHDL.
3	To represent the different digital blocks in verilog and VHDL in all available styles of modeling

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	After completion of this course the students will be able to understand.	K2
CO2	Different modeling styles available in VHDL and Verilog and difference between them	K2
CO3	Difference between verilog and VHDL	K2
CO4	Representation of different digital modules in different modeling styles available in VHDL and Verilog	K2

COURSE CONTENT

Using VHDL or Verilog do the following experiments

1. Design of 4-bit adder / subtractor
2. Design of Booth Multiplier
3. Design of 4-bit ALU
4. Design SISO, SIPO, PISO, PIPO Registers
5. Design of Ripple, Johnson and Ring counters
6. Design of MIPS processor
7. Design of Washing machine controller
8. Design of Traffic Light Controller
9. Design “1010” pattern detector using Mealy state Machine
10. Design “1100” recursive pattern detector using Moore state Machine
11. Design simple Security System Using FSM/ASM
12. Mini Project

Tools Required: VHDL or VERILOG

Hardware Required: Computers with latest Configuration

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SYLLABUS

M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

VLSI Design Laboratory –I

Course Category	Professional Core	**Course Code**	
Course Type	Laboratory	**L-T-P-C**	4-0-0-2
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OBJECTIVES: The objectives of the course are to	
1	The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/ Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate.
2	Synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/ FPGA kits)..
3	The students are required to acquire the knowledge in both the Platforms (Xilinx and Mentor graphics) by perform at least FIVE experiments on each Platform.

COURSE CONTENT

List of Experiments:

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter
4. Single Port Synchronous RAM.
5. Synchronous FIFO.
6. ALU.
7. UART Model.
8. Dual Port Asynchronous RAM.
9. Fire Detection and Control System using Combinational Logic circuits.
10. Traffic Light Controller using Sequential Logic circuits
11. Pattern Detection using Moore Machine.
12. Finite State Machine(FSM) based logic circuit.

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mento Graphics- Precision RTL

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

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SYLLABUS

M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

Writing Skills For Research Paper

Course Category	Audit Course	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	It is expected that the students should have good communication skills, proficiency in basic English, Science and good writing skills.	**Continuous Internal Assessment** **Semester End Examination** **Total Marks**	**40** **60** **100**

COURSEOBJECTIVES: The objectives of the course are to	
1	To identify and use appropriate research resources, including books, articles, and websites.
2	To evaluate the credibility of information sources.
3	To write a clear and concise research question.
4	To organize their research findings in a logical and persuasive way.
5	To use correct grammar and punctuation in documenting their sources correctly.

COURSEOUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Analyse and interpret data by using data to write clear, concise technical reports, research articles and practice professional writing style	K3&K4
CO2	Understand and apply an appropriate plan, assemble a protocol, writing task and perform original research with ethics.	K2
CO3	Identify and apply the proper methods to do to the literature and scope of the research work plan.	K2
CO4	Demonstrate improved writing skills and apply to reflect the growth in writing and communicate outcomes of the research effectively.	K3
CO5	Apply the proper methodology for writing the research reports making use of appropriate phrases.	K3

K1-Remembering, K2-Understanding, K3-Applying, K4-Analyzing, K5-Evaluating, K6-Creating

Contribution of Course Outcomes towards achievement of Program Outcomes (1– Low,2 -Medium, 3– High)

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3		2							2	
CO2		2	2	2							2	
CO3	3	3										
CO4	3	3	2	3								
CO5		3									1	

COURSE CONTENT

UNIT – I:

Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness, Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising.

UNIT – II:

Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT – III:

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

UNIT – IV:

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, and skills are needed when writing the Conclusions.

UNIT – V:

Useful phrases, how to ensure paper is as good as it could possibly be the first time submission.

TEXT BOOKS:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books).
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press.

REFERENCE BOOKS:

1.Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
2. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

WEB REFERENCES:

1. https://www.scribbr.com/category/research-paper/
2. https://www.grammarly.com/blog/how-to-write-a-research-paper/
3. https://archive.nptel.ac.in/courses/110/105/110105091/
4. **https://nptel.ac.in/courses/110105091**

SYLLABUS

M.Tech I Year I Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

Sanskrit for Technical Knowledge

Course Category	Audit Course	**Course Code**	
Course Type	Theory	**L-T-P-C**	2-0-0-2
Prerequisites		**Continuous Internal Assessment** **Semester End Examination** **Total Marks**	**40** **60** **100**

COURSEOBJECTIVES: The objectives of the course are to	
1	To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2	LearningofSanskrittoimprovebrainfunctioning
3	LearningofSanskrittodevelopthelogicinmathematics,science&othersubjects enhancingthememorypower
5	TheengineeringscholarsequippedwithSanskritwillbeabletoexplorethe Hugeknowledgefromancientliterature

COURSEOUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Demonstrate basic Sanskrit language	K2
CO2	Illustrate Ancient Sanskrit literature about science & technology	K2
CO3	Buildalogicallanguagewillhelptodeveloplogicinstudents	K6

K1-Remembering, K2-Understanding, K3-Applying, K4-Analyzing, K5-Evaluating, K6-Creating

Contribution of Course Outcomes towards achievement of Program Outcomes (1– Low,2 -Medium, 3– High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1												
CO2												
CO3												

COURSE CONTENT

UNIT – I
Alphabets in Sanskrit, Past / Present / Future Tense

UNIT – II
SimpleSentencesforminginSanskrit.

UNIT–III:
OrderofSanskritsentences,IntroductionofrootsinSanskritlanguage.

UNIT–IV:
TechnicalinformationaboutSanskritLiterature.

UNIT–V:
Technical concepts of Engineering-Electrical, Mechanical, Architecture,Mathematics.

Text Books :

1. Abhyaspustakam– Dr.Vishwas, 1st Edition, Samskrita-BhartiPublication, New Delhi
2. TeachYourselfSanskrit,PrathamaDeeksha,VempatiKutumbshastri,RashtriyaSanskritSansthanam,NewDelhiPublication
3. India's Glorious Scientific Tradition,1st Edition, SureshSoni,Oceanbooks(P)Ltd.,NewDelhi

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SYLLABUS

M.Tech I Year II Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

LOW POWER VLSI DESIGN

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment**	40
		Semester End Examination	60
		Total Marks	100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Understand the basic concept of VLSI technologies	K3
CO2	Study the Architectural Level Approach for MOS Transistor	K2
CO3	Design the Adder circuit using CMOS technologies	K3
CO4	Design the Different multiplier algorithm	K3
CO5	Understand the basic concept of Memory technologies.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3	2	2	1	0	0	0	0	0	0	0
CO2	2	3	2	2	2	0	0	0	0	0	0	0
CO3	3	2	3	2	2	0	0	0	0	0	0	0
CO4	2	2	2	2	1	0	0	0	0	0	0	0
CO5	3	2	2	2	2	0	0	1	0	0	0	0

COURSE CONTENT

UNIT I

Fundamentals of Low Power VLSI Design Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II

Low-Power Design Approaches Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT III

Low-Voltage Low-Power Adders Introduction, Standard Adder Cells, CMOS Adder‟s Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT IV

Low-Voltage Low-Power Multipliers Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT V

Low-Voltage Low-Power Memories Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS	
1.	CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011
2.	Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.
REFERENCE BOOKS	
1.	Low Power CMOS Design –AnanthaChandrakasan, IEEE Press/Wiley International, 1998
2.	Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000
3.	Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002
4.	Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995
WEB RESOURCES	

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SYLLABUS

M.Tech I Year II Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

EMBEDDED SYSTEM DESIGN

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	List technologies, their integration, design flow and software development for Embedded systems	K3
CO2	Classify embedded processors, memory and its management, embedded input and output components, Bus integration and performance	K2
CO3	Summarize device drivers, Multitasking, process, i/o and file management; middleware and application software	K3
CO4	Explain Embedded system design and development, downloading and debugging	K3
CO5	Demonstrate Case studies like Power PC, Micro blaze, NIOS-II; design on Altera platform	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3				2							2
CO2	3				2							2
CO3	3				2							2
CO4	3	2		2	2							2
CO5	**3**	2		1	2							2

COURSE CONTENT

UNIT I

Introduction An Embedded System-Definition, Examples, Current Technologies, Integration in system Design, Embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts

UNIT II

Embedded Hardware Embedded hardware building blocks, Embedded Processors – ISA architecture models, Internal processor design, processor performance, Board Memory – ROM, RAM, Auxiliary Memory, Memory Management of External Memory, Board Memory and performance.

Embedded board Input / output – Serial versus Parallel I/O, interfacing the I/O components, I/O components and performance, Board buses – Bus arbitration and timing, Integrating the Bus with other board components, Bus performance

UNIT III

Embedded Software Device drivers, Device Drivers for interrupt-Handling, Memory device drivers, On-board bus device drivers, Board I/O drivers, Explanation about above drivers with suitable examples.

Embedded operating systems – Multitasking and process Management, Memory Management, I/O and file system management, OS standards example – POSIX, OS performance guidelines, Board support packages, Middleware and Application Software – Middle ware, Middleware examples, Application layer software examples

UNIT IV

Embedded System Design, Development, Implementation and Testing Embedded system design and development lifecycle model, creating an embedded system architecture, introduction to embedded software development process and tools- Host and Target machines, linking and locating software, Getting embedded software into the target system, issues in Hardware-Software design and co-design. Implementing the design-The main software utility tool, CAD and the hardware, Translation tools, Debugging tools, testing on host machine, simulators, Laboratory tools, System Boot-Up.

UNIT V

Embedded System Design Case Studies Case studies Processor design approach of an embedded system– Power PC Processor based and Micro Blaze Processor based Embedded system design on Xilinx platform-NiosII Processor based Embedded system design on Altera platform Respective Processor architectures should be taken into consideration while designing an Embedded System

TEXT BOOKS	
1.	Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications,2005
2.	Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware / Software Introduction", John Wily & SonsInc.2002.
REFERENCE BOOKS	
1.	Peter Marwedel, "Embedded System Design", Science Publishers,2007.
2.	Arnold S Burger, "Embedded System Design", CMP,2001
3.	Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition,2008
WEB RESOURCES	
1.	https://www.digimat.in/nptel/courses/video/106105159/L01.html
2.	https://www.coursera.org/learn/introduction-embedded-systems

PRAGATI ENGINEERING COLLEGE: SURAMPALEM

R24

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DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS

M.Tech I Year II Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

SOFT COMPUTING TECHNIQUES

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	Artificial Intelligence	**Internal Assessment**	40
		Semester End Examination	60
		Total Marks	100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Identify and describe soft computing techniques and their roles in building intelligent machines	K3
CO2	To familiarize with neural networks and learning methods for neural networks	K2
CO3	To introduce the ideas of fuzzy sets, fuzzy logic and fuzzy inference system	K3
CO4	Analyze the genetic algorithms to combinatorial optimization problems	K3
CO5	Apply neural networks to pattern classification and regression problems	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	1	1									
CO2	3	1	1			1						
CO3	3	1	1			1						
CO4	3	1	1			1						
CO5	**3**	1	1			1						

COURSE CONTENT

UNIT I

Introduction: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT II

Artificial Neural Networks: Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT III

Fuzzy Logic System: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system

UNIT IV

Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and anD-colony search techniques for solving optimization problems.

UNIT V

Applications: GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems

TEXT BOOKS	
1.	Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999
2.	Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994
REFERENCE BOOKS	
1.	Fuzzy Sets, Uncertainty and Information - Klir G.J. &Folger T.A., Prentice-Hall of India Pvt. Ltd., 1993
2.	Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994
3.	Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers
4.	Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi
5.	Elements of Artificial Neural Networks - KishanMehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International
6.	Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education
7.	Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi
WEB RESOURCES	
1.	https://nptel.ac.in/courses/106105173/
2.	https://nptel.ac.in/courses/106105173/2
3.	https://nptel.ac.in/courses/106105173/14
4.	https://nptel.ac.in/courses/106105173/16
5.	https://nptel.ac.in/courses/106105173/34

SYLLABUS

M.Tech I Year II Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

DIGITAL SIGNAL PROCESSORS & ARCHITECTURS

Course Category	Professional Core	**Course Code**	
Course Type	Theory (Elective-III)	**L-T-P-C**	3-0-0-3
Prerequisites	Basics Of Digital Signal processors & Architectures	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Learn to represent real world signals in digital format and understand transform-domain (Fourier and z-transforms) representation of the signals	K3
CO2	Know to apply the linear systems approach to signal processing problems using high-level programming language	K2
CO3	Learn the basic architecture of microprocessors and digital signal processors	K3
CO4	Provide the basic knowledge of different DSP Processors	K3
CO5	Interfacing Memory and I/O Peripherals to different Programmable DSP Devices	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)											
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3	2	2	1	0	0	0	1	0	0	1
CO2	2	3	2	2	2	0	0	0	1	0	0	2
CO3	3	2	3	2	2	0	0	0	1	0	0	1
CO4	2	2	2	2	1	0	0	0	1	0	0	1
CO5	**3**	2	2	2	2	0	0	1	0	0	0	1

COURSE CONTENT

UNIT I

Introduction to Digital Signal Processing Introduction, a Digital signal processing system, the sampling process, discrete time sequences.

Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time- invariant systems, Digital filters, Decimation and interpolation. Computational Accuracy in DSP Implementations Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter

UNIT II

Architectures for Programmable DSP Devices Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing

UNIT III

Programmable Digital Signal Processors Commercial Digital signal processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors

UNIT IV

Analog Devices Family of DSP Devices Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP- 2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals

UNIT V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS	
1.	Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004
2.	A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3.	Embedded Signal Processing with the Micro Signal Architecture: Woon-SengGan, Sen M. Kuo, Wiley-IEEE Press, 2007
REFERENCE BOOKS	
1.	Digital Signal Processors, Architecture, Programming and ApplicationsB. Venkataramani and M. Bhaskar, 2002, TMH.
2.	DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co
3.	Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
4.	The Scientist and Engineer‟s Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997

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DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

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M.Tech I Year II Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

CAD FOR VLSI

Course Category	Professional Core	**Course Code**	
Course Type	Theory (Elective-III)	**L-T-P-C**	3-0-0-3
Prerequisites	ECAD	**Internal Assessment**	40
		Semester End Examination	60
		Total Marks	100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	understand the trends in physical and VLSI design cycles.	K3
CO2	analyze the partitioning, floor planning, pin assignment andplacement.	K2
CO3	understand various routing and routing algorithms.	K3
CO4	apply partitioning and routing for various models.	K3
CO5	understand concepts of chip input and output circuits.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create'.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	3									
CO2	3	3	2									
CO3	3	2	3									
CO4	3	3	3									
CO5	3	3	2									

COURSE CONTENT

UNIT I

VLSI Physical Design Automation : VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles;

UNIT II

Partitioning, Floor Planning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms

UNIT III

Global Routing and DetailedRouting :Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms

UNIT IV

Physical Design Automation of FPGAs and MCMs:FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model;

Introduction to MCM Technologies, MCM Physical Design Cycle

UNIT V

ESD Protection, Input Circuits, Output Circuits and L (di/dt) noise, On-chip clock Generation and Distribution, Latch-up and its prevention

TEXT BOOKS	
1.	Algorithms for VLSI Physical Design Automation by NaveedShervani, 3rd Edition, 2005, Springer International Edition
2.	CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011
REFERENCE BOOKS	
1.	VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific
2.	Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd
3.	VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition
WEB RESOURCES	
1.	https://www.youtube.com/watch?v=zOkxhERkWy0
2.	https://www.youtube.com/watch?v=jZ6LAcHmvng
3.	https://www.youtube.com/watch?v=rck5O8DnWlg

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SYLLABUS

M.Tech I Year II Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

SYSTEM ON CHIP DESIGN

Course Category	Professional Core	**Course Code**	
Course Type	Theory (Elective-IV)	**L-T-P-C**	3-0-0-3
Prerequisites	Basics of chip design	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Able to understand System Architecture.	K3
CO2	Able to unnderstand Basic concepts in Processor Architecture.	K2
CO3	Able to understand SOC Memory System.	K3
CO4	Able to understand Customization and Configuration.	K3
CO5	Able to understand Design and evaluation .	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3	2	2	2	1	0	0	1	2	1	1
CO2	2	2	2	3	2	2	0	0	1	2	1	1
CO3	3	3	2	2	3	1	0	0	1	1	1	1
CO4	2	2	2	2	2	1	0	0	0	2	1	1
CO5	**2**	3	2	2	2	2	0	0	1	1	1	1

COURSE CONTENT

UNIT I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity

UNIT II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors

UNIT III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction

UNIT IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism

UNIT V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression

TEXT BOOKS	
1.	Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, WileyIndia Pvt.Ltd,2011
2.	ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional
REFERENCE BOOKS	
1.	Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2.	Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3.	System on Chip Verification – Methodologies and Techniques, Paterson and Leena Singh L, 2001, Kluwer Academic Publishers
WEB RESOURCES	
1.	www.vssut.ac.in
2.	**Searchsecurity.techtarget.com**
3.	www.geeksforgeeks.com
4.	www.123seminarsonly.com
5.	**www.slideshare.net**

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DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS

M.Tech I Year II Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

CMOS MIXED SIGNAL DESIGN

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	VLSI design and Analog VLSI Design	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Understand the Switched capacitors Circuits and Operation and Analysis	K3
CO2	Understand the Operation and Analysis of PLLS	K2
CO3	To know Data Converter Fundamentals, Nyquist Rate D/A Converters	K3
CO4	To explain Data Converter Fundamentals, Nyquist Rate A/D Converters	K3
CO5	To analyze the Oversampling Converters and Continuous-Time Filters	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	1	1									1
CO2	3	1	1									1
CO3	3	1	1									1
CO4	3	1	1									1
CO5	**3**	1	1									1

COURSE CONTENT

UNIT I

Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT II

Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT III

Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT IV

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time interleaved converters.

UNIT V

Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibitquantizers, Delta sigma D/A

TEXT BOOKS	
1.	Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition,2002
2.	CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition,2010
3.	Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition,2013
REFERENCE BOOKS	
1.	CMOS Integrated Analog-to- Digital and Digital-to-Analog convertersRudy Van De Plassche, Kluwer Academic Publishers,2003
2.	Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005
3.	CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009
WEB RESOURCES	
1.	https://www.youtube.com/watch?v=PhTU4pbWMEQ&list=PLLDC70psjvq5vtrb0EdII4xIKA15ec-Ij&index=10&t=0s
2.	https://www.youtube.com/watch?v=7xVSL93ZZq8&list=PLLDC70psjvq5vtrb0EdII4xIKA15ec-Ij&index=15
3.	https://www.youtube.com/watch?v=WjtUpOPEljQ&list=PLLDC70psjvq5vtrb0EdII4xIKA15ec-Ij&index=20

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DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS

M.Tech I Year II Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

Embedded System Design Laboratory

Course Category	Professional Core	**Course Code**	
Course Type	Laboratory	**L-T-P-C**	4-0-0-2
Prerequisites	**ARM-926 with PERFECT RTOS And** ARM-CORTEX processor using any open source RTOS	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	To understand to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits andARM-Cortex.	
CO2	To develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification	
CO3	The programs developed for the implementation should be at the level of an embedded systemdesign.	
CO4	nplement the interfacing of display with the ARM- CORTEXprocessor.	
CO5	Different design platforms used for an embedded systems applications	

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	1	1	0	0	0	0	0	0	0	0
CO2	3	2	1	2	0	0	0	0	0	0	0	0
CO3	3	2	1	1	0	0	0	0	0	0	0	0
CO4	3	2	1	1	0	0	0	0	0	0	0	0
CO5	3	3	1	1	0	0	0	0	0	0	0	0

COURSE CONTENT

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.
9. Implement the interfacing of display with the ARM- CORTEX processor.
10. Interface ADC and DAC ports with the Input and Output sensitive devices.
11. Simulate the temperature DATA Logger with the SERIAL communication with PC.
12. Implement the developer board as a modem for data communication using serial port communication between two PC's.

SYLLABUS

M.Tech I Year II Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

VLSI Design Laboratory –II

Course Category	Professional Core	**Course Code**	
Course Type	Laboratory	**L-T-P-C**	4-0-0-2
Prerequisites		**Internal Assessment**	40
		Semester End Examination	60
		Total Marks	100

COURSE CONTENT

The students are required to design and implement the Layout of the following Experiments of any SIX using CMOS 130nm Technology with Mentor Graphics Tool.

List of Experiments:

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Static RAM Cell.
6. Dynamic RAM Cell.
7. ROM
8. Digital-to-Analog-Converter.
9. Analog-to-Digital Converter.

PART-B: Mixed Signal Simulation

The students are required to perform the following experimental concepts with suitable complexity mixed-signal application based circuits of any FOUR (circuits consisting of both analog and digital parts) using necessary software tools.

1. List of experimental Concepts:
2. Analog circuit simulation.
3. Digital circuit simulation.
4. Mixed signal simulation.
5. Layout Extraction.
6. Parasitic values estimation from layout.
7. Layout Vs Schematic.
8. **Net List Extraction.**
9. **Design Rule Checks.**

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool, Mixed Signal simulator

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits

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PedagogyStudies

Course Category	Audit Course	**Course Code**	
Course Type		**L-T-P-C**	2-0-0-2
Prerequisites		**Continuous Internal Assessment** **Semester End Examination** **Total Marks**	**40** **60** **100**

COURSEOBJECTIVES: The objectives of the course are to	
1	ReviewexistingevidenceonthereviewtopictoinformprogrammedesignandpolicymakingundertakenbytheDfID,otheragenciesandresearchers.
2	Identifycriticalevidencegapstoguidethedevelopment.

COURSEOUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Whatpedagogicalpracticesarebeingusedbyteachersinformalandinformalclassroomsindevelopingcountries?	K1
CO2	What is the evidence on the effectiveness of these pedagogicalpractices,inwhatconditions,andwithwhatpopulationoflearners?	K1
CO3	Howcanteachereducation(curriculumandpracticum)andtheschoolcurriculumandguidancematerialsbestsupport effectivepedagogy?	K1

K1-Remembering, K2-Understanding, K3-Applying, K4-Analyzing, K5-Evaluating, K6-Creating

Contribution of Course Outcomes towards achievement of Program Outcomes (1– Low,2 -Medium, 3– High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1												
CO2												
CO3												

COURSE CONTENT

UNIT – I
:IntroductionandMethodology: Aimsandrationale,Policybackground,Conceptualframeworkandterminology,Theoriesoflearning,Curriculum,Teachereducation,Conceptualframework,Researchquestions**,**OverviewofmethodologyandSearching.

UNIT – II :Thematic overview: Pedagogical practices are being used by teachersin formal and informal classrooms in developing countries, Curriculum, Teachereducation.

UNIT–III : Evidenceontheeffectivenessofpedagogicalpractices:Methodology for the in depth stage: quality assessment of included studies, Howcan teacher education (curriculum and practicum) and the school curriculumandguidancematerialsbestsupporteffectivepedagogy,Theoryofchange,Strength and nature of the body of evidence for effective pedagogical practices,Pedagogictheoryandpedagogicalapproaches,Teachers'attitudesandbeliefs andPedagogicstrategies.

UNIT–IV: Professionaldevelopment:Alignmentwithclassroompracticesandfollow-upsupport,Peersupport,Supportfromtheheadteacherand thecommunity,Curriculumandassessment,Barrierstolearning: limited resourcesandlargeclasssizes

UNIT–V: Researchgapsandfuturedirections:Researchdesign,Contexts,Pedagogy, Teacher education, Curriculum and assessment, Dissemination andresearchimpact.

Text Books :
1. ClassroominteractioninKenyanprimaryschools,AckersJ,HardmanF,Compare,31(2):245-261,2001
2. Curricularreforminschools:Theimportanceofevaluation,AgrawalM,JournalofCurriculumStudies,36(3):361-379,2004

ReferenceBooks:
Teacher training in Ghana: does it count? Multi-site teacher educationresearch project (MUSTER) country report 1, Akyeampong K, London:DFID,2003

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DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS

M.Tech I Year II Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

PersonalityDevelopmentthrough LifeEnlightenmentSkills

Course Category	Audit Course	**Course Code**	
Course Type		**L-T-P-C**	2-0-0-0
Prerequisites		**Continuous Internal Assessment** **Semester End Examination** **Total Marks**	

COURSEOBJECTIVES: The objectives of the course are to	
1	To learn to achieve the highest goal happily.
2	To become a person with stable mind, pleasing personality and determination
3	To Awaken wisdom in students

COURSEOUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	StudyofShrimad-Bhagwad-Geetawillhelpthestudentindevelopinghispersonalityandachievethehighestgoalinlife	K2
CO2	ThepersonwhohasstudiedGeetawillleadthenationandmankindtopeaceandprosperity	K3
CO3	StudyofNeetishatakamwillhelpindevelopingversatilepersonalityofstudents.	K5

K1-Remembering, K2-Understanding, K3-Applying, K4-Analyzing, K5-Evaluating, K6-Creating

Contribution of Course Outcomes towards achievement of Program Outcomes (1– Low,2 -Medium, 3– High)												
CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1												
CO2												
CO3												

COURSE CONTENT

UNIT – I :
Neetisatakam-Holisticdevelopmentofpersonality,Verses-19,20,21,22(wisdom),Verses-29,31,32(pride&heroism),Verses-26,28,63,65(virtue),
Verses-52,53,59(don'ts),Verses-71,73,75,78(do's)
.

UNIT – II :
Approachtodaytodayworkandduties.ShrimadBhagwadGeeta:Chapter2-Verses41,47,48

UNIT–III :
Chapter3-Verses13,21,27,35,Chapter6-Verses5,13,17,23,35,
Chapter18-Verses45,46,48

UNIT–IV:
Statementsofbasicknowledge.
ShrimadBhagwadGeeta:Chapter2-Verses56,62,68
Chapter12-Verses13,14,15,16,17,18

UNIT–V:
PersonalityofRolemodel.ShrimadBhagwadGeeta:Chapter2-Verses17,Chapter3-Verses36,37,42,
Chapter4-Verses18,38,39
Chapter18–Verses37,38,63

Text Books :
Srimad Bhagavad Gita, Swami Swarupananda Advaita Ashra(PublicationDepartment),Kolkata
2. Bhartrihari'sThreeSatakam(Niti-sringar-vairagya),P.Gopinath

ReferenceBooks:
RashtriyaSanskritSansthanam,NewDelhi

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DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS

M.Tech I Year III Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

TESTING AND TESTABILITY

Course Category	Professional Core	**Course Code**	
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	Basic knowledge of testing and state machines	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Remember the basic concepts of Analog and Digital testing devices used in chip designing	K3
CO2	Understand the concepts of simulation and design verification used in chip modeling	K2
CO3	Apply the concept of testing digital circuits used in industrial applications	K3
CO4	Analyze the build in self test testing procedures used in chip manufacturing	K3
CO5	Design TAP controllers used in testing process using BDSL	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	2	3	1	2		3				2	1
CO2	2	1	3	1	2		1				2	2
CO3	2	2	3	2	1		2				2	3
CO4	2	2	3	1	2		1				2	2
CO5	2	2	3	1	1		3				2	2

COURSE CONTENT

UNIT I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault

UNIT II

Logic and Fault Simulation : Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation

UNIT III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan

UNIT IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per- Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST

UNIT V

Boundary Scan Standard : Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions

TEXT BOOKS	
1.	**Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits -** M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers
2.	
REFERENCE BOOKS	
1.	Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, JaicoPublishingHouse
2.	Digital Circuits Testing and Testability - P.K. Lala, AcademicPress
WEB RESOURCES	
1.	

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SYLLABUS

M.Tech I Year III Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

SEMICONDUCTOR MEMORY DESIGN AND TESTING

Course Category	Professional Core	**Course Code**	
Course Type	Theory (Elective-IV)	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment**	40
		Semester End Examination	60
		Total Marks	100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Understand different types of RAM, ROM designs.	K3
CO2	Analyze different RAM and ROM architectures and interconnects.	K2
CO3	Implement fault models for memory testing.	K3
CO4	Analyze different memory testing and design for testability.	K3
CO5	Design reliable memories with efficient architecture to improve processes times and power.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	1	3	3	0	0	0	0	0	0	0	0	2
CO2	1	3	2	0	0	0	0	0	0	0	0	1
CO3	2	3	1	0	0	0	0	0	0	0	0	1
CO4	0	3	3	0	0	0	0	0	0	0	0	2
CO5	**1**	3	2	0	0	0	0	0	0	0	0	1

COURSE CONTENT

UNIT I

Random Access Memory Technologies SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT II

Non-volatile Memories Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT IV

Semiconductor Memory Reliability and Radiation Effects General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT V

Advanced Memory Technologies and High-density Memory Packing Technologies Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS	
1.	Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley
2.	Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma-2002
REFERENCE BOOKS	
1.	Modern Semiconductor Devices for Integrated Circuits – ChenmingCHu, 1st Ed., Prentice Hall
WEB RESOURCES	
1.	https://www.electronics-notes.com/articles/electronic_components/semiconductor
2.	https://www.electronicproducts.com/Digital_ICs/Memory/Fundamentals_of_nonvolatile_memory
3.	https://link.springer.com/content/pdf/bbm%3A978-0-306-47972-4%2F1.pdf
4.	https://www.researchgate.net/publication/220649285_Memory_Fault_Modeling
5.	https://catalogimages.wiley.com/images/db/pdf/0471208132.excerpt.pdf

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SYLLABUS

M.Tech I Year III Semester **R24** **Specialization: VLSI SYSTEM DESIGN**

VLSI SIGNAL PROCESSING

Course Category	Professional Core	**Course Code**	
Course Type	Theory (Elective-III)	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Design Low Power IIR Filter Using Pipelining And Parallel Processing	K3
CO2	Analyze Folding Techniques For Area Reduction	K2
CO3	Understand VLSI Design Methodology For Signal Processing Systems	K3
CO4	Understand VLSI Algorithms And Architectures For DSP.	K3
CO5	Implement Basic Architectures For DSP Using CAD Tools	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3	2	1	0	0	0	0	0	0	0	1
CO2	2	3	3	0	0	0	0	0	0	0	0	1
CO3	2	3	3	0	0	0	0	0	0	0	0	0
CO4	2	3	2	0	0	0	0	0	0	0	0	0
CO5	**2**	2	2	0	0	0	0	0	0	0	0	0

COURSE CONTENT

UNIT I

Introduction to DSP Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT II

Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multi rate systems Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT III

Systolic Architecture Design Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT IV

Fast Convolution Introduction – Cook-Toom Algorithm – Wino gard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT V

Low Power Design Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS	
1.	VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley InterScience
2.	VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, PrenticeHall
REFERENCE BOOKS	
1.	Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall
2.	VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY),USA
WEB RESOURCES	
1.	https://www.slideshare.net/krishna602/ds-p-algorithms-02
2.	https://www.semanticscholar.org/paper/Folding-and-Register-Minimization-Transformation
3.	https://www.oreilly.com/library/view/vlsi-digital-signal/9780471241867/sec-7.2.html
4.	https://www.scribd.com/doc/58450407/COOK-TOOM-ALGORITHM
5.	https://ieeexplore.ieee.org/document/860100