

**PRAGATI ENGINEERING COLLEGE: SURAMPALEM
(AUTONOMOUS)
M.Tech II Semester Regular/Supplementary Examinations, July – 2024**

**DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(VLSISD)**

Time: 3 hours

Max. Marks: 60

**Answer any FIVE questions
All questions carry EQUAL marks**

5X12=60

Q.NO.		Question	BTL	CO	Marks
1.	a.	Explain about Decimation and interpolation.	K2	CO1	6M
	b.	Discuss about A/D Conversion errors.	K4	CO1	6M
2.	a.	Explain the computational building blocks of DSP with neat sketch.	K2	CO2	6M
	b.	Briefly discuss about Speed Issues.	K2	CO2	6M
3	a.	Briefly discuss about the floating point and block diagram of floating point formats	K2	CO3	6M
	b.	Discuss in brief about the data addressing capabilities of programmable DSP devices with examples.	K4	CO3	6M
4	a.	Build and explain the basic Architecture of ADSP 2100.	K3	CO4	6M
	b.	Explain the following i). Basic Peripherals ii). Arithmetic Unit	K2	CO4	6M
5.		Discuss about the following i). Parallel I/O interface ii). External bus interfacing signals	K4	CO2	12M
6.	a	Explain about Data Addressing modes of TMS320C54XX	K2	CO3	6M
	b	Explain about On-Chip Peripherals of TMS320C54XX	K2	CO3	6M
7	a	How the shifters are useful in DSP? Explain the functionality of barrel shifter	K1	CO4	6M
	b	Explain in detail about Black fin processor	K2	CO4	6M
8	a	Discuss about Features for External interfacing	K2	CO2	6M
	b	How does DMA help in increasing the processing speed of a DSP processor	K1	CO5	6M