

PRAGATI ENGINEERING COLLEGE: SURAMPALEM
(AUTONOMOUS)
M.Tech II Semester Regular/Supplementary Examinations, July – 2024

SYSTEM ON-CHIP DESIGN
(VLSI SD)

Time: 3 hours

Max. Marks: 60

Answer any FIVE questions
 All questions carry EQUAL marks

5X12=60

Q.NO.		Question	BTL	CO	Marks
1.	a.	Explain the processor architecture and its implementation with neat sketch.	K2	CO1	6M
	b.	Explain briefly about the components required for the system design.	K2	CO1	6M
2.	a.	Explain about processor Selection for SOC.	K2	CO2	6M
	b.	Explain the architecture of Superscalar Processors.	K2	CO2	6M
3.	a.	With a neat diagram explain set associate cache and fully associative cache?	K2	CO3	6M
	b.	Discuss SOC memory systems.	K1	CO3	6M
4.	a.	Describe the Architecture of customizing instruction processor.	K2	CO4	6M
	b.	Explain the basic bus physical structure?	K2	CO4	6M
5.	a.	Discuss the application study of JPEG compression.	K1	CO5	6M
	b.	Discuss the SOC design approach.	K1	CO5	6M
6.	a.	Draw and explain the system-on-chip design flow diagram?	K2	CO1	6M
	b.	Explain Memory addressing of SOC design.	K2	CO1	6M
7.	a.	Explain briefly about multi-level cache.	K2	CO3	6M
	b.	Brief overview of SOC external memory and Internal Memory.	K1	CO3	6M
8.	a.	Explain the concept of Customizable Soft Processor with suitable example.	K2	CO4	6M
	b.	Explain the concept of AMBA standard bus.	K2	CO4	6M