

PRAGATI ENGINEERING COLLEGE: SURAMPALEM
(AUTONOMOUS)
M.Tech II Semester Regular/Supplementary Examinations, July – 2024

CMOS DIGITAL IC DESIGN
(VLSI SD)

Time: 3 hours

Max. Marks: 60

Answer any FIVE questions
All questions carry EQUAL marks

5X12=60

Q.NO.		Question	BTL	CO	Marks
1.	a.	Describe about the following i). Transient response ii). Rise Time iii). Fall Time	K2	CO1	6M
	b.	Discuss about CMOS Inverter logic with neat sketch	K2	CO1	6M
2.		Design and implement CMOS full adder circuit	K4	CO2	12M
3	a.	Discuss about behavior of Bistable elements of Sequential MOS Logic Circuits	K2	CO3	6M
	b.	Construct the D latch by using CMOS logic and explain its operation in detail	K3	CO3	6M
4	a.	Describe about Synchronous dynamic pass transistor circuits	K2	CO4	6M
	b.	Explain about basic principle of Dynamic Logic Circuits	K2	CO4	6M
5.	a.	Distinguish the performance of SRAM and DRAM	K4	CO5	6M
	b.	Write about Leakage currents in DRAM cell	K3	CO5	6M
6.		Realize CMOS complex logic gates using the Boolean function $Z=A(D+C)+BE$	K4	CO2	12M
7	a	Design an NAND gate using Transmission gate Logic	K4	CO2	6M
	b	Explain about Pseudo NMOS logic gates	K2	CO1	6M
8		Outline different types of RAM cells. Draw and explain the operation of a single bit dynamic RAM cell.	K2	CO5	12M