

**PRAGATI ENGINEERING COLLEGE: SURAMPALEM
(AUTONOMOUS)**

M.Tech II Semester Regular/Supplementary Examinations, July – 2024

**CMOS MIXED SIGNAL CIRCUIT DESIGN
(VLSI SD)**

Time: 3 hours

Max. Marks: 60

**Answer any FIVE questions
All questions carry EQUAL marks**

5X12=60

Q.NO.		Question	BTL	CO	Marks
1.	a.	Discuss about basic building blocks of Switched Capacitor.	K2	CO1	6M
	b.	If $C_1 = C_2 = C$, find the value of C that will emulate a $1M\Omega$ resistor if the clock frequency is 200 KHz.	K3	CO1	6M
2.	a.	Explain about Non ideal effects in PLLs.	K2	CO2	6M
	b.	Discuss about Basic PLL topology.	K2	CO2	6M
3	a.	What are the dynamic characteristics that influence the performance of DACs ?	K1	CO3	6M
	b.	Design a decoder based DAC with a detailed explanation.	K4	CO3	6M
4	a.	Explain in detail about Interpolating A/D converters	K2	CO4	6M
	b.	Explain the static and dynamic characteristics of ADCs.	K2	CO4	6M
5.	a.	Discuss about Delta sigma modulators with multibit quantizers.	K2	CO5	6M
	b.	What is a flash converter? Explain the function of a 3 bit flash ADC.	K1	CO5	6M
6.	a	What are biquad filters? Explain about the two switched capacitor biquad realizations.	K1	CO1	6M
	b	Design a switched capacitor realization for a first order, high pass circuit with a high frequency gain of -10 and a -3dB frequency of 1 kHz using a clock of 100kHz.	K4	CO1	6M
7		Distinguish between oversampling without noise shaping and with noise shaping	K4	CO5	12M
8	a	Explain about Folding A/D converters	K2	CO4	6M
	b	Discuss about Delay locked loops	K2	CO2	6M