

**PRAGATI ENGINEERING COLLEGE: SURAMPALEM  
(AUTONOMOUS)**

**M.Tech II Semester Regular/Supplementary Examinations, July – 2024**

**LOW POWER VLSI DESIGN  
(VLSI SD)**

Time: 3 hours

Max. Marks: 60

**Answer any FIVE questions  
All questions carry EQUAL marks**

Q.NO.		Question	BTL	CO	Marks
1.	a.	What are the Low-Voltage, Low-Power design considerations? Explain	K2	CO1	6M
	b.	Obtain the relation of static power consumption and leakage currents in CMOS	K3	CO1	6M
2.	a.	Compare Voltage scaling, Variable Threshold and Multi Threshold techniques for Low Power applications.	K2	CO2	6M
	b.	Compare pipe lining and parallel processing with an example	K2	CO2	6M
3	a.	Provide the low power strategy for 1 bit adder cell suitable examples.	K2	CO3	6M
	b.	Provide the Power requirements for 2 bit RCA, CLA and CSA cells.	K3	CO3	6M
4	a.	Illustrate the power consumption for Wallace tree and Array multipliers.	K2	CO4	6M
	b.	Detail the spurious power suppression in multipliers.	K2	CO4	6M
5.	a.	Compare SRAM and DRAM memories in Portable devices	K2	CO5	6M
	b.	Provide the differences between 6T and 4T static RAM cells	K2	CO5	6M
6.	a	Derive the short circuit current and illustrate its effect on channel length modulation.	K3	CO1	6M
	b	Explain the causes of punch through and its effects in CMOS.	K2	CO1	6M
7	a	Explain the necessity of two-dimensional decoding mechanism in memories.	K2	CO5	6M
	b	Discuss any two types of low voltage low power logic styles.	K2	CO2	6M
8	a	Write down the algorithm of Baugh-Wooley multiplier and illustrate with an example.	K2	CO3	6M
	b	Brief the Trends of Technology and Power Supply Voltage	K2	CO1	6M