

**PRAGATI ENGINEERING COLLEGE: SURAMPALEM
(AUTONOMOUS)**

II B.Tech II Semester Regular/Supplementary Examinations, May-2024

**DIGITAL IC APPLICATIONS
(ECE)**

Time: 3 hours

Max. Marks: 70

Answer ONE Question from each Unit

All Questions Carry Equal Marks

Q. No.	Questions	BTL	CO	Marks
UNIT – I				
1.	a) Explain the VHDL Styles of Modeling with an example.	K1	CO1	7M
	b) Discuss the VHDL Operators with suitable examples.	K2	CO1	7M
OR				
2.	a) Explain the Verilog HDL Data Types with an example.	K2	CO1	7M
	b) Describe the if-else and case-end case statement with suitable examples.	K2	CO1	7M
UNIT – II				
3.	a) Write the VHDL code for carry look ahead adder by using behavioral style of modeling.	K1	CO2	7M
	b) Describe the multiplexer diagram using IC 74X151. List the applications of multiplexers.	K2	CO2	7M
OR				
4.	a) Write the VHDL code for priority encoder by using behavioral style of modeling.	K2	CO2	7M
	b) Explain the operation for BCD to Gray code converter circuit with suitable VHDL Code.	K3	CO2	7M
UNIT – III				
5.	a) Describe the operation of ring counter with neat diagram and timing waveforms.	K4	CO3	7M
	b) Write the VHDL Code for the synchronous counter with its timing waveform.	K2	CO3	7M
OR				
6.	a) Describe the SISO and SIPO right shift operation with example data of Q 3 Q 2 Q 1 Q 0 =1111.	K2	CO3	7M
	b) Write the VHDL Code for ripple counter with its timing waveform.	K3	CO3	7M
UNIT – IV				
7.	a) Draw the CMOS 2 input NOR gate and explain its operation with a truth table.	K3	CO4	7M
	b) Explain the one bit full-adder circuit with a gate level schematic.	K2	CO4	7M
OR				
8.	a) Draw the NMOS 2 -input NAND gate with depletion NMOS as a load and explain its operation.	K3	CO5	7M
	b) What is pseudo-nMOS logic? Realize the following expression, $Z = ((A+B+C)(D+E)(F))'$ using pseudo-nMOS logic.	K2	CO5	7M
UNIT – V				
9.	a) Draw the CMOS SR latch circuit based on NOR2 gates and explain its operation in detail.	K3	CO5	7M
	b) Draw the gate-level schematic of the clocked NOR-based JK latch circuit and explain its operation.	K3	CO5	7M
OR				
10.	a) Draw the CMOS implementation of the D-latch and explain it in detail.	K2	CO1	7M
	b) Explain the operation modes of the transistors in the NOR-based CMOS SR latch circuit.	K2	CO1	7M