

**PRAGATI ENGINEERING COLLEGE: SURAMPALEM  
(AUTONOMOUS)**

**II B.Tech II Semester Regular/Supplementary Examinations, May-2024**

**COMPUTER ORGANIZATION**

**(Common to CSE(AI&ML), CSE(AI) and CSE(DS))**

**Time: 3 hours**

**Max. Marks: 70**

**Answer ONE Question from each Unit**

**All Questions Carry Equal Marks**

Q. No.	Questions	BTL	CO	Marks
<b>UNIT – I</b>				
1.	a) Describe the functions of the main hardware components of a general purpose computer.	K2	CO1	7M
	b) Subtract (136) <sub>8</sub> from (636) <sub>8</sub> using 8's complement method.	K3	CO1	7M
<b>OR</b>				
2.	a) Draw and explain the flow chart for fixed point division algorithm	K3	CO1	7M
	b) Solve (+21) <sub>10</sub> + (-16) <sub>10</sub> and (-23) <sub>10</sub> + (+13) <sub>10</sub> arithmetic operations using 2's complement representation for negative numbers	K3	CO1	7M
<b>UNIT – II</b>				
3.	a) List and explain various micro operations with their hardware representations	K1	CO2	7M
	b) Discuss about bus and memory transfer.	K2	CO2	7M
<b>OR</b>				
4.	a) What is the role of Stack data structure in computer architecture? Explain the PUSH and POP instructions	K3	CO2	7M
	b) What is an Instruction format? Explain about various basic computer instruction formats.	K2	CO2	7M
<b>UNIT – III</b>				
5.	a) Explain about reduced instruction set computer	K2	CO3	7M
	b) Explain about address sequencing	K2	CO3	7M
<b>OR</b>				
6.	a) Discuss the three main types of Data Transfer and Manipulation instructions	K2	CO3	7M
	b) With neat diagram, explain the address selection for control memory.	K2	CO3	7M
<b>UNIT – IV</b>				
7.	a) Give the details of memory hierarchy? Explain how the data Transfer is done between memory and the processor?	K2	CO4	7M
	b) List and explain about various types of asynchronous data transfer	K1	CO4	7M
<b>OR</b>				
8.	a) Describe the characteristics of Cache memory. Explain Write-through and Writeback methods.	K2	CO4	7M
	b) Discuss various possible modes of Data transfer to and from the peripherals in a computer system	K3	CO4	7M
<b>UNIT – V</b>				
9.	a) Explain the phases of Instruction pipeline with a neat flow chart.	K2	CO5	7M
	b) Discuss various hardware implementations of Inter-processor synchronization	K3	CO5	7M
<b>OR</b>				
10.	a) Explain about the array processor.	K2	CO5	7M
	b) In how many ways multi processors can be connected internally? Draw each interconnection structure.	K1	CO5	7M