

PRAGATI ENGINEERING COLLEGE: SURAMPALEM
(AUTONOMOUS)
II B.Tech II Semester Regular/Supplementary Examinations, May-2024
DIGITAL ELECTRONICS
(EEE)

Time: 3 hours

Max. Marks: 70

Answer ONE Question from each Unit
All Questions Carry Equal Marks

Q. No.	Questions	BTL	CO	Marks
UNIT – I				
1.	a) Perform the subtraction using 1's complement and 2's complement methods. i) 11010 – 10000 ii) 11010 – 1101 iii) 100 – 110000	K2	CO1	7M
	b) How are negative numbers represented? Represent signed numbers from +7 to -8 using different ways of representation	K2	CO1	7M
OR				
2.	a) Reduce using mapping the following expression and implement the real minimal expression in Universal logic. $F = \sum m(0, 2, 4, 6, 7, 8, 10, 12, 13, 15)$	K2	CO1	7M
	b) List out the basic theorems and properties of Boolean Algebra.	K3	CO1	7M
UNIT – II				
3.	a) Perform the realization of half adder and full adder using decoders and logic gates.	K2	CO2	7M
	b) Design a 4 bit combinational logic to subtract one bit from the other. Draw the logic diagram using NAND and NOR Gates	K2	CO2	7M
OR				
4.	a) Express the following functions in SOP and POS forms: i) $F(A,B,C,D) = \sum(2, 4, 7, 10, 12, 14)$ ii) $F(x,y,z) = \pi(3, 5, 7)$.	K3	CO2	7M
	b) Explain about a full adder using two half adders.	K2	CO2	7M
UNIT – III				
5.	a) Implement the following multiple output combinational logic circuit using a 4 line to 16 line decoder: $F1 = \sum m(0, 1, 4, 7, 12, 14, 15)$ $F3 = \sum m(2, 3, 7, 8, 10)$ $F2 = \sum m(1, 3, 6, 9, 12)$ $F4 = \sum m(1, 3, 5)$	K2	CO3	7M
	b) Discuss a few applications of multiplexers and distinguish between a multiplexer and a decoder.	K2	CO3	7M
OR				
6.	a) Realize the function $f(A,B,C,D) = \sum(1,2,5,8,10,14) + d(6,7,15)$ using i) 8:1 MUX ii) 4:1 MUX	K3	CO3	7M

	b)	Draw a block diagram of a PLA and explain it's architecture. Write differences between PLA and PROM. What is the design procedure of a PLA based circuit?	K3	CO3	7M																																							
UNIT – IV																																												
7.	a)	Draw the circuit diagram of a positive edge triggered JK flip flop and explain its operation with the help of a truth table?	K3	CO4	7M																																							
	b)	Convert a D flip flop into SR flip flop and JK flip flop?	K2	CO4	7M																																							
OR																																												
8.	a)	Design a 4-bit universal shift register using D flip flops and multiplexers?	K3	CO4	7M																																							
	b)	Explain the operation of 4-bit ring counter with circuit diagram, state transition diagram and state table. Draw the corresponding timing diagrams?	K2	CO4	7M																																							
UNIT – V																																												
9.	a)	What is the importance of reduction of number of states? What is the advantage of standard form for state tables? Explain with an example.	K2	CO5	7M																																							
	b)	A synchronous counter is controlled by two input signals A and B. The counter does not operate, if A = 0 and B = 0. When A = 0 and B = 1, the counter operates as a mod four counter. If A=1 and B=0 the counter operates as a mod eight counter. Draw an FSM chart and design a circuit.	K4	CO5	7M																																							
OR																																												
10.	a)	Design Finite State machine for the state table using JK Flip-Flop. <table border="1" data-bbox="339 1167 1013 1518"><thead><tr><th rowspan="2">Present state (Q_1Q_0)</th><th colspan="4">Inputs (AB)</th></tr><tr><th>00</th><th>01</th><th>10</th><th>11</th></tr></thead><tbody><tr><td>00</td><td>01</td><td>00</td><td>00</td><td>01</td></tr><tr><td>01</td><td>10</td><td>00</td><td>00</td><td>10</td></tr><tr><td>10</td><td>11</td><td>00</td><td>00</td><td>11</td></tr><tr><td>11</td><td>01</td><td>00</td><td>00</td><td>01</td></tr></tbody></table> <table border="1" data-bbox="585 1460 1013 1518"><tr><td colspan="5">Next State ($Q_1^*Q_0^*$)</td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table>	Present state (Q_1Q_0)	Inputs (AB)				00	01	10	11	00	01	00	00	01	01	10	00	00	10	10	11	00	00	11	11	01	00	00	01	Next State ($Q_1^*Q_0^*$)										K3	CO5	7M
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	b)	Why state reduction is necessary in sequential circuit design? What are the different methods of state reduction? Explain implication table method of state reduction with an example.	K3	CO5	7M																																							