

**PRAGATI ENGINEERING COLLEGE: SURAMPALEM**  
(AUTONOMOUS)

**II B.Tech I Semester Supplementary Examinations, June - 2024**

**SWITCHING THEORY AND LOGIC DESIGN**  
(ECE)

Time: 3 hours

Max. Marks: 70

**Answer ONE Question from each Unit**  
**All Questions Carry Equal Marks**

Q. No.	Questions	BTL	CO	Marks
<b>UNIT – I</b>				
1.	a) Encode the message bits (1110) <sub>2</sub> into 7-bit even parity hamming code	K2	CO1	7M
	b) Perform the following arithmetic using 2's complement method. i) 101111-100110 ii) 111001-011010	K2	CO1	7M
<b>OR</b>				
2.	a) Convert the following expression into sum of products and product of sums. $X'+X(X+Y')(Y+Z')$	K2	CO1	7M
	b) Implement the following Boolean function with NAND gates only. $F(X, Y, Z) = \sum m(1, 2, 3, 4, 5, 7)$	K2	CO1	7M
<b>UNIT – II</b>				
3.	a) Simplify the following function using K-Map method $F(A,B,C,D) = \sum(0,1,2,3,4,6,9,10) + d(7,11,12,13,15)$	K2	CO2	7M
	b) Design a code converter that converts a decimal digit from the 8,4,2,1 code to BCD	K2	CO2	7M
<b>OR</b>				
4.	a) Minimise on the map the five variable function. $F = \sum m(0, 1, 4, 5, 6, 13, 14, 15, 22, 24, 25, 28, 29, 30, 31)$ .	K2	CO2	7M
	b) Reduce the following function using K-map $F = \prod M(1, 4, 5, 6, 7, 8, 9, 14, 15, 22, 23, 24, 25, 28, 29, 30, 31)$	K2	CO2	7M
<b>UNIT – III</b>				
5.	a) Tabulate the PLA programming table for the four Boolean functions listed below and minimize the number of product terms. $A(x, y, z) = \sum(1, 2, 4, 6)$ ; $B(x, y, z) = \sum(0, 1, 6, 7)$ ; $C(x, y, z) = \sum(2, 6)$ ; $D(x, y, z) = \sum(1, 2, 3, 5, 7)$ .	K4	CO3	7M
	b) Explain the internal structure of PLA.	K3	CO3	7M
<b>OR</b>				
6.	a) Design a switching circuit that converts a 4-bit binary code into a 4-bit gray code using ROM array.	K4	CO3	7M
	b) Explain briefly about logic construction of 32x4 ROM.	K3	CO3	7M

UNIT – IV																																																						
7.	a)	Explain the analysis procedure for asynchronous sequential circuits	K3	CO4	7M																																																	
	b)	Design Mod-12 synchronous counter using J-K or T flip-flops.	K4	CO4	7M																																																	
OR																																																						
8.	a)	Draw the logic diagram of a 4-bit binary ripple counter using positive edge triggering.	K3	CO4	7M																																																	
	b)	What is a shift register. Explain the working of serial in-serial out shift register with logic diagram and wave forms	K3	CO4	7M																																																	
UNIT – V																																																						
9.	a)	Using State reduction technique reduce the state table given below and tabulate the reduced state table. <table border="1"><thead><tr><th rowspan="2">PS</th><th colspan="2">NS</th><th colspan="2">Output</th></tr><tr><th>x=0</th><th>x=1</th><th>x=0</th><th>x=1</th></tr></thead><tbody><tr><td>A</td><td>A</td><td>B</td><td>0</td><td>0</td></tr><tr><td>B</td><td>C</td><td>D</td><td>0</td><td>0</td></tr><tr><td>C</td><td>A</td><td>D</td><td>0</td><td>0</td></tr><tr><td>D</td><td>E</td><td>F</td><td>0</td><td>1</td></tr><tr><td>E</td><td>A</td><td>F</td><td>0</td><td>1</td></tr><tr><td>F</td><td>E</td><td>F</td><td>0</td><td>1</td></tr></tbody></table>	PS	NS		Output		x=0	x=1	x=0	x=1	A	A	B	0	0	B	C	D	0	0	C	A	D	0	0	D	E	F	0	1	E	A	F	0	1	F	E	F	0	1	K4	CO5	7M										
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b)	Compare between Mealy and Moore Finite state machine (FSM)	K3	CO5	7M																																																		
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10.	a)	Reduce the number of states in the following state table using an State reduction technique and tabulate the reduced state-table. <table border="1"><thead><tr><th rowspan="2">PS</th><th colspan="2">NS</th><th colspan="2">Output</th></tr><tr><th>x=0</th><th>x=1</th><th>x=0</th><th>x=1</th></tr></thead><tbody><tr><td>A</td><td>F</td><td>B</td><td>0</td><td>0</td></tr><tr><td>B</td><td>D</td><td>C</td><td>0</td><td>0</td></tr><tr><td>C</td><td>F</td><td>E</td><td>0</td><td>0</td></tr><tr><td>D</td><td>G</td><td>A</td><td>1</td><td>0</td></tr><tr><td>E</td><td>D</td><td>C</td><td>0</td><td>0</td></tr><tr><td>F</td><td>F</td><td>B</td><td>1</td><td>1</td></tr><tr><td>G</td><td>G</td><td>H</td><td>0</td><td>1</td></tr><tr><td>H</td><td>G</td><td>A</td><td>1</td><td>0</td></tr></tbody></table>	PS	NS		Output		x=0	x=1	x=0	x=1	A	F	B	0	0	B	D	C	0	0	C	F	E	0	0	D	G	A	1	0	E	D	C	0	0	F	F	B	1	1	G	G	H	0	1	H	G	A	1	0	K4	CO5	7M
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b)	Explain the procedure for state minimization using merger graph and merger table.	K3	CO5	7M																																																		