COURSE STRUCTURE AND SYLLABUS

For

M. Tech

VLSI SYSTEM DESIGN

(Applicable for batches admitted from 2019-2020)

Learning is Supreme Deity

PRAGATI ENGINEERING COLLEGE

(Autonomous)

Permanently Affiliated to JNT University Kakinada and Approved by AICTE, New Delhi,
Accredited by NAAC with "A" Grade
Recognized by UGC 2(f) and 12(b) under UGC act, 1956
1-378, ADB Road, Surampalem – 533 437, Near Peddapuram, E.G.Dist., A.P.

PRAGATI ENGINEERING COLLEGE: SURAMPALEM

(Autonomous)

VLSI SYSTEM DESIGN

I Semester

Sub Code	Name of the Subject	L	P	C
19041T01	Digital System Design	3		3
19041T02	VLSI Technology and Design	3		3
19041T03	CMOS Analog IC Design	3		3
19041D01 19041D02 19041D03	Elective I 1. Digital Design using HDL 2. Advanced Operating Systems 3. Soft Computing Techniques	3		3
19041D04 19041D05 19041D06	Elective II 1. CPLD and FPGA Architectures and Applications 2. Advanced Computer Architecture 3. Hardware Software Co-Design	3		3
16041L01	Laboratory VLSI Laboratory-I	-	4	2
Total				**17**

II Semester

Sub Code	Name of the Subject	L	P	C
19042T04	CMOS Mixed Signal Circuit Design	3		3
19042T05	CMOS Digital IC Design	3		3
19042T06	Low Power VLSI Design	3		3
19042D07 19042D08 19042D09	Elective III 1. CAD for VLSI 2. DSP Processors & Architectures 3. VLSI Signal Processing	3		3
19042D10 19042D11 19042D12	Elective IV 1. System on Chip Design 2. Optimization Techniques in VLSI Design 3. Semiconductor Memory Design and Testing	3		3
19042L02	Laboratory VLSI Laboratory-II	-	4	2
Total				17

PRAGATI ENGINEERING COLLEGE: SURAMPALEM

(Autonomous)

III Semester

Sub Code	Name of the Subject	L	P	C
19043T07	Embedded System Design	3		3
19043T08	Testing and Testability	3		3
19043C01	Comprehensive Viva-Voce	--	--	3
19043S01	Seminar – I			2
19043P01	Project Work Part - I			6
Total				17

IV Semester

Sub Code	Name of the Subject	L	P	C
19044S02	Seminar – II			2
19044P02	Project Work Part - II			15
Total				17

The project will be evaluated at the end of the IV Semester

DIGITAL SYSTEM DESIGN
I M. Tech I Semester

Course Category	Professional Core	**Course Code**	19041T01
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Analyse various Minimization Procedures for minimizing Switching functions and Camp Algorithms.	K4
CO2	Design PLD's & PLA by using Minimization and Folding Algorithms	K3
CO3	Design the Large-Scale Digital Systems	K3
CO4	Analyse the Fault Diagnosis in Combinational Circuits.	K4
CO5	Discuss the Fault Diagnosis in Sequential Circuits and its Experiments.	K2

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2										
CO2	3	2	2									
CO3	3	1	3									
CO4	3	3										
CO5	3	1	1									

COURSE CONTENT	
UNIT I	Minimization Procedures and CAMP Algorithm: Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.
UNIT II	PLA Design, Minimization and Folding Algorithms: Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.
UNIT III	Design of Large Scale Digital Systems: Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT IV	Fault Diagnosis in Combinational Circuits: Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.
UNIT V	Fault Diagnosis in Sequential Circuits: Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS	
1.	Logic Design Theory-N. N. Biswas, PHI,1993.
2.	Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001,TMH
3.	Digital system Design usingPLDd-Lala,2003
REFERENCE BOOKS	
1.	Fundamentals of Logic Design – Charles H. Roth, 5th Ed., CengageLearning.
2.	Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & SonsInc,2003
WEB RESOURCES	

VLSI TECHNOLOGY ANDDESIGN
I M. Tech I Semester

Course Category	Professional Core	**Course Code**	19041T02
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	MOSFET construction and working, combinational	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Demonstrate IC design rules, parameters and design techniques of combinational and sequential systems	K3
CO2	Illustrate fabrication processes of NMOS, PMOS, CMOS and outline VLSI design issues	K2
CO3	Infer electrical properties and scaling of MOS circuits	K3
CO4	Analyze switch, gate logic and clocked sequential circuits, design ALU subsystem	K3
CO5	Summarize floor planning, Architecture -RT design, Low power architectures and their testing, chip design methodologies	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2										3
CO2	3											2
CO3	3											2
CO4	3	2										2
CO5	3											2

COURSE CONTENT	
UNIT I	**VLSI Technology:** Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters. VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues
UNIT II	**CMOS VLSI Design:** MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies, comparison of different processes. **Building Blocks of a VLSI circuit:** Computer architecture, memory architectures, communication interfaces, mixed signal interfaces. **VLSI Design Issues:** Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.
UNIT III	Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitatitive and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT IV	**Subsystem Design and Layout:** Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations. Subsystem Design Processes: Some general considerations and an illustration of design processes, design of an ALU subsystem.
UNIT V	**Floor Planning:** Introduction, Floor planning methods, off-chip connections. **Architecture Design:** Introduction, Register-Transfer design, high-level synthesis, architectures for low power, architecture testing. **Chip Design:** Introduction and design methodologies.

TEXT BOOKS	
1.	Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, SholehEshraghian, 2005, PHI Publications.
2.	Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.
3.	VLSI Design-Dr.K.V.K.K.Prasad, KattulaShyamala, Kogent Learning Solutions Inc
REFERENCE BOOKS	
1.	VLSI Design Technologies for Analog and Digital Circuits
2.	Introduction to VLSI Systems: A Logic
3.	Principals of CMOS VLSI Design-N.H.E Weste
WEB RESOURCES	
1.	https://nptel.ac.in/courses/117101058/3
2.	https://nptel.ac.in/courses/117106093/1

CMOS ANALOG IC DESIGN
I M. Tech I Semester

Course Category	Professional Core	**Course Code**	19041T03
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Understand the basic parameters of MOS transistor and different models	K3
CO2	Understand the basic theory of MOS transistors and Different characteristics'	K2
CO3	Study the Different application of C-MOS transistor	K3
CO4	Design the Op-Amps and its application using C-MOS transistor	K3
CO5	Learn the basics theory of open loop comparators.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)											
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3	2	2	1	0	0	0	0	0	0	0
CO2	2	3	2	2	2	0	0	0	0	0	0	0
CO3	3	2	3	2	2	0	0	0	0	0	0	0
CO4	2	2	2	2	1	0	0	0	0	0	0	0
CO5	3	2	2	2	2	0	0	1	0	0	0	0

COURSE CONTENT	
UNIT I	MOS Devices and Modeling The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.
UNIT II	Analog CMOS Sub-Circuits MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.
UNIT III	CMOS Amplifiers Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.
UNIT IV	CMOS Operational Amplifiers Design of CMOS Op Amps, Compensation of Op Amps, Design of Two- Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAMP.

UNIT V	Comparators Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS	
1.	CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010
2.	Analysis and Design of Analog Integrated Circuits- Paul R. Gray, PaulJ. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.
REFERENCE BOOKS	
1.	Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2.	Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3.	CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI
WEB RESOURCES	

DIGITAL DESIGN USING HDL
I M. Tech I Semester

Course Category	Professional Core	**Course Code**	19041D01
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Design the digital circuits using VHDL and Verilog HDL models.	K3
CO2	Discuss Combinational and Sequential logic Circuit Design.	K2
CO3	Design Digital circuits using Verilog HDL Behavioural modelling and compare styles of it.	K3
CO4	Describe the Synthesis of Digital logic Circuit Design and sequential circuits	K3
CO5	Implement the Testing of Digital Logic Circuits using CAD Tools.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	3	1								
CO2	3	3	2	1								
CO3	3	3	2	1								
CO4	3	3	2	1								
CO5	3	3	1	1								

COURSE CONTENT	
UNIT I	Digital Logic Design using VHDL Introduction, designing with VHDL, design entry methods, logic synthesis , entities , architecture , packages and configurations, types of models: dataflow , behavioral , structural, signals vs. variables, generics, data types, concurrent vs. sequential statements , loops and program controls. Digital Logic Design using Verilog HDL Introduction, Verilog Data types and Operators, Binary data manipulation, Combinational and Sequential logic design, Structural Models of Combinational Logic, Logic Simulation, Design Verification and Test Methodology, Propagation Delay, Truth Table models using Verilog.
UNIT II	Combinational Logic Circuit Design using VHDL Combinational circuits building blocks: Multiplexers, Decoders , Encoders , Code converters, Arithmetic comparison circuits , VHDL for combinational circuits , Adders-Half Adder, Full Adder, Ripple-Carry Adder, Carry Look-Ahead Adder, Subtraction, Multiplication. Sequential Logic Circuit Design using VHDL Flip-flops, registers & counters, synchronous sequential circuits: Basic design steps, Mealy State model, Design of FSM using CAD tools, Serial Adder Example, State Minimization, Design of Counter using sequential Circuit approach

UNIT III	Digital Logic Circuit Design Examples using Verilog HDLBehavioral modeling , Data types, Boolean-Equation-Based behavioral models of combinational logics , Propagation delay and continuous assignments, latches and level-sensitive circuits in Verilog, Cyclic behavioral models of flip-flops and latches and Edge detection, comparison of styles for behavioral model; Behavioral model, Multiplexers, Encoders and Decoders, Counters, Shift Registers, Register files, Dataflow models of a linear feedback shift register, Machines with multi cycle operations, ASM and ASMD charts for behavioral modeling, Design examples, Keypad scanner and encoder.
UNIT IV	Synthesis of Digital Logic Circuit Design Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic with latches and flip-flops, Synthesis of Explicit and Implicit State Machines, Registers and counters.
UNIT V	Testing of Digital Logic Circuits and CAD Tools Testing of logic circuits, fault model, complexity of a test set, path-sensitization, circuits with tree structure, random tests, testing of sequential circuits, built in self test, printed circuit boards, computer aided design tools, synthesis, physical design.

TEXT BOOKS	
1.	Stephen Brown & Zvonko Vranesic, "Fundamentals of Digital logic design with VHDL", Tata McGraw Hill,2nd edition
2.	Michael D. Ciletti, "Advanced digital design with the Verilog HDL", Eastern economy edition, PHI
REFERENCE BOOKS	
1.	Stephen Brown & Zvonko Vranesic, "Fundamentals of Digital logic with Verilog design", Tata McGraw Hill,2nd edition
2.	Bhaskar, "VHDL Primer",3rd Edition, PHI Publications
3.	Ian Grout, "Digital systems design with FPGAs and CPLDs", Elsevier Publications.
WEB RESOURCES	

ADVANCED OPERATING SYSTEMS
I M. Tech I Semester

Course Category	Professional Core	**Course Code**	19041D02
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	Operating Systems	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Understand the concepts of I/O function, Interrupts & Memory hierarchy in operating systems.	K2
CO2	Interpret the concept of Unix & Linux in operating systems.	K4
CO3	Perceive the concept of Pipes, FIFOs, Message queues & Semaphores.	K4
CO4	Interpret the concept of ATM networks, Client - Server model, Remote procedu call and Group communication.	K2
CO5	Perceive the concept of Clock synchronization, Bully algorithm, Ring algorithr Deadlock in distributed systems.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	1	1	1	1	2	1						2
CO2	1	1	1	1	2	1						2
CO3	1	1	1	1	2	1						2
CO4	1	1	1	1	2	1						2
CO5	1	1	1	1	2	1						2

COURSE CONTENT	
UNIT I	**Introduction to Operating Systems:** Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System
UNIT II	**Introduction to UNIX and LINUX**: Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations
UNIT III	**System Calls:** System calls and related file structures, Input / Output, Process creation & termination. Inter Process Communication: Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.
UNIT IV	**Introduction to Distributed Systems:** Goals of distributed system, Hardware and software concepts, Design issues. Communication in Distributed Systems: Layered protocols, ATM

	networks, Client - Server model, Remote procedure call and Group communication.
UNIT V	**Synchronization in Distributed Systems:** Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions Deadlocks :Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS	
1.	The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2.	Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI
3.	The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill
REFERENCE BOOKS	
1.	Operating Systems: Internal and Design Principles -Stallings, 6th Ed., PE.
2.	Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
3.	Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
4.	UNIX User Guide – Ritchie & Yates
5.	UNIX Network Programming - W.Richard Stevens, 1998, PHI
WEB RESOURCES	
1.	https://nptel.ac.in/courses/106106157/15
2.	https://nptel.ac.in/courses/106106157/13
3.	https://nptel.ac.in/courses/106106168

SOFT COMPUTING TECHNIQUES
I M. Tech I Semester

Course Category	Professional Core	**Course Code**	19041D03
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	Artificial Intelligence	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Identify and describe soft computing techniques and their roles in building intelligent machines	K3
CO2	To familiarize with neural networks and learning methods for neural networks	K2
CO3	To introduce the ideas of fuzzy sets, fuzzy logic and fuzzy inference system	K3
CO4	Analyze the genetic algorithms to combinatorial optimization problems	K3
CO5	Apply neural networks to pattern classification and regression problems	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	1	1									
CO2	3	1	1			1						
CO3	3	1	1			1						
CO4	3	1	1			1						
CO5	**3**	1	1			1						

COURSE CONTENT	
UNIT I	**Introduction:** Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.
UNIT II	**Artificial Neural Networks:** Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.
UNIT III	Fuzzy Logic System: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system

UNIT IV	**Genetic Algorithm:** Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and anD-colony search techniques for solving optimization problems.
UNIT V	**Applications:** GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems

TEXT BOOKS	
1.	Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999
2.	Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994
REFERENCE BOOKS	
1.	Fuzzy Sets, Uncertainty and Information - Klir G.J. &Folger T.A., Prentice-Hall of India Pvt. Ltd., 1993
2.	Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994
3.	Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers
4.	Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi
5.	Elements of Artificial Neural Networks - KishanMehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International
6.	Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education
7.	Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi
WEB RESOURCES	
1.	https://nptel.ac.in/courses/106105173/
2.	https://nptel.ac.in/courses/106105173/2
3.	https://nptel.ac.in/courses/106105173/14
4.	https://nptel.ac.in/courses/106105173/16
5.	https://nptel.ac.in/courses/106105173/34

CPLD AND FPGA ARCHITECURES AND APPLICATIONS
I M. Tech I Semester

Course Category	Professional Core	**Course Code**	19041D04
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	VLSI	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	understand the concepts of various PLAs and PLDs.	K3
CO2	understandFPGA Programming Technologies and its applications.	K2
CO3	analyze SRAM Programmable FPGAs and the architectures of Xilinx XC2000, XC3000 and XC4000	K3
CO4	analyze the architectures of Actel ACT1, ACT2 and ACT3.	K3
CO5	understand concepts of various Design Applications General Design Issues.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	2									
CO2	3	3	3									
CO3	3	2	3									
CO4	3	3	3									
CO5	3	2	3									

COURSE CONTENT	
UNIT I	Introduction to Programmable Logic Devices Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.
UNIT II	Field Programmable Gate Arrays Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs
UNIT III	SRAM Programmable FPGAs Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.
UNIT IV	Anti-Fuse Programmed FPGAs Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT V	Design Applications General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS	
1.	Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2.	Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.
REFERENCE BOOKS	
1.	Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India
2.	Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/ Samiha Mourad, Pearson Low Price Edition
3.	Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes
4.	FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series
WEB RESOURCES	
1.	https://www.youtube.com/watch?v=2c5dQrqhfn0
2.	https://www.youtube.com/watch?v=uEVmdvBo_lk
3.	https://www.youtube.com/watch?v=gCAYY0fHPq4

ADVANCED COMPUTER ARCHITECTURE
I M. Tech I Semester

Course Category	Professional Core	**Course Code**	19041D05
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	Basics of advanced computer architeture	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Discuss the organisation of computer-based systems and how a range of design choices are influenced by applications	K3
CO2	Understand different processor architectures and system-level design processes.	K2
CO3	Understand the components and operation of a memory hierarchy and the range of performance issues influencing its design.	K3
CO4	Understand the organisation and operation of current generation parallel computer systems, including multiprocessor and multicore systems.	K3
CO5	Develop systems programming skills in the content of computer system design and organisation.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	2	2	2	2	0	0	0	2	0	0	1
CO2	2	3	2	3	2	0	0	0	1	0	0	2
CO3	2	2	2	3	2	0	0	0	1	0	0	1
CO4	2	3	2	2	3	0	0	0	1	0	0	1
CO5	**3**	2	3	2	2	0	0	1	1	0	0	1

COURSE CONTENT	
UNIT I	Fundamentals of Computer Design Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl‟slaw. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, Operations in the instruction set.

UNIT II	Pipelines Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.
UNIT III	Instruction Level Parallelism (ILP)-The Hardware Approach Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo‟s approach, Branch prediction, High performance instruction delivery- Hardware based speculation. ILP Software Approach Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.
UNIT IV	Multi Processors and Thread Level Parallelism Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.
UNIT V	Inter Connection and Networks Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS	
1.	John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier,2002
2.	
REFERENCE BOOKS	
1.	John P. Shen and Miikko H. Lipasti - Modern Processor Design : Fundamentals of Super ScalarProcessors,2013
2.	Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill,1984
3.	Advanced Computer Architecture - A Design Space Approach -Dezso Sima, Terence Fountain, Peter Kacsuk , PearsonEd,1997
WEB RESOURCES	
1.	http://scitechconnect.elsevier.com/category/computer-science/
2.	https://www.sztaki.hu/en/science/departments/lpds
3.	http://www.ecs.umass.edu/ece/koren/arith/
4.	https://onlinelibrary.wiley.com/doi/full/10.1002/9780470050118.ecse071
5.	

HARDWARE SOFTWARE CO-DESIGN
I M. Tech I Semester

Course Category	Professional Core	**Course Code**	19041D06
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	acquire the knowledge about system specification and modeling.	K2
CO2	learn the formulation of partitioning the hardware and software	K2
CO3	analyze about the hardware and software integration	K2
CO4	study the hardware design languages and its components	K2
CO5	formulate the design specification and module creation	K2

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	2	1	1								
CO2	3	2	2	1								
CO3	3	3	2	1								
CO4	3	2	1	1								
CO5	3	3	3	1								

COURSE CONTENT	
UNIT I	**Co- Design Issues:** Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.
UNIT II	**Prototyping and Emulation:** Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.
UNIT III	Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.
UNIT IV	Design Specification and Verification: Design, co-design, the codesign computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT V	Languages for System – Level Specification and Design-I: System level specification, design representation for system level synthesis, system level specification languages. Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS	
1.	Hardware / Software Co- Design Principles and Practice – JorgenStaunstrup, Wayne Wolf – 2009, Springer.
2.	Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers
REFERENCE BOOKS	
1.	A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer Publications.
2.	
WEB RESOURCES	

VLSI Design Laboratory -I
I M. Tech I Semester

Course Category	Professional Core	**Course Code**	16041L01
Course Type	Laboratory	**L-T-P-C**	4-0-0-2
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

- The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/ Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate
- synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/ FPGA kits).
- The students are required to acquire the knowledge in both the Platforms (Xilinx and Mentor graphics) by perform at least FIVE experiments on each Platform.

List of Experiments:

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter
4. Single Port Synchronous RAM.
5. Synchronous FIFO.
6. ALU.
7. UART Model.
8. Dual Port Asynchronous RAM.
9. Fire Detection and Control System using Combinational Logic circuits.
10. Traffic Light Controller using Sequential Logic circuits
11. Pattern Detection using Moore Machine.
12. Finite State Machine(FSM) based logic circuit.

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mento Graphics-Precision RTL

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

CMOS MIXED SIGNAL CIRCUIT DESIGN
I M. Tech II Semester

Course Category	Professional Core	**Course Code**	19042T04
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	VLSI design and Analog VLSI Design	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Understand the Switched capacitors Circuits and Operation and Analysis	K3
CO2	Understand the Operation and Analysis of PLLS	K2
CO3	To know Data Converter Fundamentals, Nyquist Rate D/A Converters	K3
CO4	To explain Data Converter Fundamentals, Nyquist Rate A/D Converters	K3
CO5	To analyze the Oversampling Converters and Continuous-Time Filters	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	1	1									1
CO2	3	1	1									1
CO3	3	1	1									1
CO4	3	1	1									1
CO5	**3**	1	1									1

COURSE CONTENT	
UNIT I	Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.
UNIT II	Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications
UNIT III	Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters
UNIT IV	Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time interleaved converters.
UNIT V	Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS	
1.	Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition,2002
2.	CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition,2010
3.	Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition,2013
REFERENCE BOOKS	
1.	CMOS Integrated Analog-to- Digital and Digital-to-Analog convertersRudy Van De Plassche, Kluwer Academic Publishers,2003
2.	Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005
3.	CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009
WEB RESOURCES	
1.	https://www.youtube.com/watch?v=PhTU4pbWMEQ&list=PLLDC70psjvq5vtrb0EdII4xIKA15ec-Ij&index=10&t=0s
2.	https://www.youtube.com/watch?v=7xVSL93ZZq8&list=PLLDC70psjvq5vtrb0EdII4xIKA15ec-Ij&index=15
3.	https://www.youtube.com/watch?v=WjtUpOPEljQ&list=PLLDC70psjvq5vtrb0EdII4xIKA15ec-Ij&index=20

CMOS DIGITAL IC DESIGN
I M. Tech II Semester

Course Category	Professional Core	**Course Code**	19042T05
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	Basic knowledge in VLSI and Mos transistors concepts	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Remember the basic concepts of NMOS logic and inverter devices used in portable consumer devices	K3
CO2	Understand the design of transmission gated used to implement analog switches and multiplexers	K2
CO3	Apply the MOS logic and concept of flip flops for sequential circuits used temporary storage of data or delay signals	K3
CO4	Analyze dynamic logic circuits used in temporary storage of signal using various load capacitances.	K3
CO5	Compare different type of memory devices used for storage	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	2	2	1	2		1				2	1
CO2	1	1	3	1	2		1				2	2
CO3	1	2	3	2	2		1				2	1
CO4	2	2	2	1	2		1				2	2
CO5	**1**	2	3	1	1		1				2	1

COURSE CONTENT	
UNIT I	MOS Design Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic**.**
UNIT II	Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.
UNIT III	Sequential MOS Logic Circuits Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop
UNIT IV	Dynamic Logic Circuits Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT V	Semiconductor MemoriesTypes, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXT BOOKS	
1.	Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2.	CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.
REFERENCE BOOKS	
1.	Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2.	Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI
WEB RESOURCES	

LOW POWER VLSI DESIGN
I M. Tech II Semester

Course Category	Professional Core	**Course Code**	19042T06
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Understand the basic concept of VLSI technologies	K3
CO2	Study the Architectural Level Approach for MOS Transistor	K2
CO3	Design the Adder circuit using CMOS technologies	K3
CO4	Design the Different multiplier algorithm	K3
CO5	Understand the basic concept of Memory technologies.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3	2	2	1	0	0	0	0	0	0	0
CO2	2	3	2	2	2	0	0	0	0	0	0	0
CO3	3	2	3	2	2	0	0	0	0	0	0	0
CO4	2	2	2	2	1	0	0	0	0	0	0	0
CO5	3	2	2	2	2	0	0	1	0	0	0	0

COURSE CONTENT	
UNIT I	Fundamentals of Low Power VLSI Design Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.
UNIT II	Low-Power Design Approaches Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches System Level Measures, Circuit Level Measures, Mask level Measures.
UNIT III	Low-Voltage Low-Power Adders Introduction, Standard Adder Cells, CMOS Adder‟s Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.
UNIT IV	Low-Voltage Low-Power Multipliers Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT V	Low-Voltage Low-Power Memories Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS	
1.	CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011
2.	Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.
REFERENCE BOOKS	
1.	Low Power CMOS Design –Anantha Chandrakasan, IEEE Press/Wiley International, 1998
2.	Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000
3.	Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002
4.	Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995
WEB RESOURCES	
1.	
2.	
3.	
4.	
5.	

CAD FOR VLSI
I M. Tech II Semester

Course Category	Professional Core	**Course Code**	19042D07
Course Type	Theory (Elective-III)	**L-T-P-C**	3-0-0-3
Prerequisites	ECAD	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	understand the trends in physical and VLSI design cycles.	K3
CO2	analyze the partitioning, floor planning, pin assignment andplacement.	K2
CO3	understand various routing and routing algorithms.	K3
CO4	apply partitioning and routing for various models.	K3
CO5	understand concepts of chip input and output circuits.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	3	3									
CO2	3	3	2									
CO3	3	2	3									
CO4	3	3	3									
CO5	3	3	2									

COURSE CONTENT	
UNIT I	**VLSI Physical Design Automation** : VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles;
UNIT II	Partitioning, Floor Planning, Pin Assignment and Placement:Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms
UNIT III	Global Routing and DetailedRouting :Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms
UNIT IV	**Physical Design Automation of FPGAs and MCMs:**FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model;

	Introduction to MCM Technologies, MCM Physical Design Cycle
UNIT V	ESD Protection, Input Circuits, Output Circuits and L (di/dt) noise, On-chip clock Generation and Distribution, Latch-up and its prevention

TEXT BOOKS	
1.	Algorithms for VLSI Physical Design Automation by NaveedShervani, 3rd Edition, 2005, Springer International Edition
2.	CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011
REFERENCE BOOKS	
1.	VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific
2.	Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd
3.	VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition
WEB RESOURCES	
1.	https://www.youtube.com/watch?v=zOkxhERkWy0
2.	https://www.youtube.com/watch?v=jZ6LAcHmvng
3.	https://www.youtube.com/watch?v=rck5O8DnWlg
4.	
5.	

DIGITAL SIGNAL PROCESSORS & ARCHITECTURS
I M. Tech II Semester

Course Category	Professional Core	**Course Code**	19042D08
Course Type	Theory (Elective-III)	**L-T-P-C**	3-0-0-3
Prerequisites	Basics Of Digital Signal processors & Architectures	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Learn to represent real world signals in digital format and understand transform-domain (Fourier and z-transforms) representation of the signals	K3
CO2	Know to apply the linear systems approach to signal processing problems using high-level programming language	K2
CO3	Learn the basic architecture of microprocessors and digital signal processors	K3
CO4	Provide the basic knowledge of different DSP Processors	K3
CO5	Interfacing Memory and I/O Peripherals to different Programmable DSP Devices	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3	2	2	1	0	0	0	1	0	0	1
CO2	2	3	2	2	2	0	0	0	1	0	0	2
CO3	3	2	3	2	2	0	0	0	1	0	0	1
CO4	2	2	2	2	1	0	0	0	1	0	0	1
CO5	**3**	2	2	2	2	0	0	1	0	0	0	1

COURSE CONTENT	
UNIT I	Introduction to Digital Signal Processing Introduction, a Digital signal processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time- invariant systems, Digital filters, Decimation and interpolation. Computational Accuracy in DSP Implementations Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter
UNIT II	Architectures for Programmable DSP Devices Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing
UNIT III	Programmable Digital Signal Processors Commercial Digital signal processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX

	Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors
UNIT IV	Analog Devices Family of DSP Devices Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP- 2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals
UNIT V	Interfacing Memory and I/O Peripherals to Programmable DSP Devices Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS	
1.	Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004
2.	A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3.	Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007
REFERENCE BOOKS	
1.	Digital Signal Processors, Architecture, Programming and ApplicationsB. Venkataramani and M. Bhaskar, 2002, TMH.
2.	DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co
3.	Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
4.	The Scientist and Engineer‟s Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997
WEB RESOURCES	
1.	https://www.arm.com/resources/education/online-courses/digital-signal-processing
2.	https://electronicsforu.com/resources/cool-stuff-misc/8-free-digital-signal-processing-ebooks
3.	https://www.analog.com/en/design-center/landing-pages/001/beginners-guide-to-dsp.html
4.	http://users.ece.utexas.edu/~bevans/hp-dsp-seminar/
5.	

VLSI SIGNAL PROCESSING
I M. Tech II Semester

Course Category	Professional Core	**Course Code**	19042D09
Course Type	Theory (Elective-III)	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Design Low Power IIR Filter Using Pipelining And Parallel Processing	K3
CO2	Analyze Folding Techniques For Area Reduction	K2
CO3	Understand VLSI Design Methodology For Signal Processing Systems	K3
CO4	Understand VLSI Algorithms And Architectures For DSP.	K3
CO5	Implement Basic Architectures For DSP Using CAD Tools	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3	2	1	0	0	0	0	0	0	0	1
CO2	2	3	3	0	0	0	0	0	0	0	0	1
CO3	2	3	3	0	0	0	0	0	0	0	0	0
CO4	2	3	2	0	0	0	0	0	0	0	0	0
CO5	**2**	2	2	0	0	0	0	0	0	0	0	0

COURSE CONTENT	
UNIT I	Introduction to DSPTypical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques
UNIT II	Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multi rate systems Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding
UNIT III	Systolic Architecture Design Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays
UNIT IV	Fast Convolution Introduction – Cook-Toom Algorithm – Wino gard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT V	Low Power Design Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS	
1.	VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley InterScience
2.	VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, PrenticeHall
REFERENCE BOOKS	
1.	Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall
2.	VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY),USA
WEB RESOURCES	
1.	https://www.slideshare.net/krishna602/ds-p-algorithms-02
2.	https://www.semanticscholar.org/paper/Folding-and-Register-Minimization-Transformation
3.	https://www.oreilly.com/library/view/vlsi-digital-signal/9780471241867/sec-7.2.html
4.	https://www.scribd.com/doc/58450407/COOK-TOOM-ALGORITHM
5.	https://ieeexplore.ieee.org/document/860100

SYSTEM ON CHIP DESIGN
I M. Tech II Semester

Course Category	Professional Core	**Course Code**	19042D10
Course Type	Theory (Elective-IV)	**L-T-P-C**	3-0-0-3
Prerequisites	Basics of chip design	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Able to understand System Architecture.	K3
CO2	Able to unnderstand Basic concepts in Processor Architecture.	K2
CO3	Able to understand SOC Memory System.	K3
CO4	Able to understand Customization and Configuration.	K3
CO5	Able to understand Design and evaluation .	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	3	2	2	2	1	0	0	1	2	1	1
CO2	2	2	2	3	2	2	0	0	1	2	1	1
CO3	3	3	2	2	3	1	0	0	1	1	1	1
CO4	2	2	2	2	2	1	0	0	0	2	1	1
CO5	**2**	3	2	2	2	2	0	0	1	1	1	1

COURSE CONTENT	
UNIT I	Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity
UNIT II	Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors
UNIT III	Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction

UNIT IV	Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism
UNIT V	Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression

TEXT BOOKS	
1.	Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, WileyIndia Pvt.Ltd,2011
2.	ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional
REFERENCE BOOKS	
1.	Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2.	Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3.	System on Chip Verification – Methodologies and Techniques, Paterson and Leena Singh L, 2001, Kluwer Academic Publishers
WEB RESOURCES	
1.	**www.vssut.ac.in**
2.	**Searchsecurity.techtarget.com**
3.	**www.geeksforgeeks.com**
4.	**www.123seminarsonly.com**
5.	**www.slideshare.net**

OPTIMIZATION TECHNIQUES IN VLSI DESIGN
I M. Tech II Semester

Course Category	Professional Core	**Course Code**	19042D11
Course Type	Theory (Elective-IV)	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Compare various statistical modelling methods such as Monte carlo techniques, Pelgroms methods, principle component based and quad tree based modelling methods.	K3
CO2	Analyze the systems by using concepts of high level and gate level statistical methods	K2
CO3	Analyze complete knowledge regarding the various algorithms used for optimization of power and area.	K3
CO4	Develop the real time applications using optimization techniques such as Genetic Algorithms.	K3
CO5	Apply CMOS technology -specific layout rules in the placement and routing of transistor sand to verify the functionality, timing and power	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	-	1	-	2	2	-	-	-	-	-	-	-
CO2	-	3	2	3	-	-	-	-	-	-	-	-
CO3	-	1	-	4	2	-	-	-	-	-	-	-
CO4	-	-	-	3	-	2	-	-	-	-	-	-
CO5	**1**	2	-	3	3	-	-	-	-	-		-

COURSE CONTENT	
UNIT I	Statistical Modeling Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom‟s model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models
UNIT II	Statistical Performance, Power and Yield Analysis Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, Highlevel statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation

UNIT III	Convex Optimization Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Polynomial fitting
UNIT IV	Genetic Algorithm Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation-Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement GASP algorithm- unified algorithm
UNIT V	FPGA Routing Procedures and Power Estimation Global routing-FPGA technology mapping-circuit generation-test generation in a FPGA frame work-test generation procedures, Power estimation-application of GA Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm

TEXT BOOKS	
1.	Statistical Analysis and Optimization for VLSI: Timing and Power -Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005
2.	Genetic Algorithm for VLSI Design, Layout and Test Automation -Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998
REFERENCE BOOKS	
1.	Convex Optimization Stephen Boyd, Lieven Vandenberghe, Cambridge University Press,2004
WEB RESOURCES	
1.	
2.	
3.	
4.	
5.	

SEMICONDUCTOR MEMORY DESIGN AND TESTING
I M. Tech II Semester

Course Category	Professional Core	**Course Code**	19042D12
Course Type	Theory (Elective-IV)	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Understand different types of RAM, ROM designs.	K3
CO2	Analyze different RAM and ROM architectures and interconnects.	K2
CO3	Implement fault models for memory testing.	K3
CO4	Analyze different memory testing and design for testability.	K3
CO5	Design reliable memories with efficient architecture to improve processes times and power.	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	1	3	3	0	0	0	0	0	0	0	0	2
CO2	1	3	2	0	0	0	0	0	0	0	0	1
CO3	2	3	1	0	0	0	0	0	0	0	0	1
CO4	0	3	3	0	0	0	0	0	0	0	0	2
CO5	**1**	3	2	0	0	0	0	0	0	0	0	1

COURSE CONTENT	
UNIT I	Random Access Memory Technologies SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM
UNIT II	Non-volatile Memories Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture
UNIT III	Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory
UNIT IV	Semiconductor Memory Reliability and Radiation Effects General reliability issues RAM

	failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures
UNIT V	Advanced Memory Technologies and High-density Memory Packing TechnologiesFerroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS	
1.	Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley
2.	Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma-2002
REFERENCE BOOKS	
1.	Modern Semiconductor Devices for Integrated Circuits – Chenming CHu, 1st Ed., Prentice Hall
2.	
WEB RESOURCES	
1.	https://www.electronics-notes.com/articles/electronic_components/semiconductor
2.	https://www.electronicproducts.com/Digital_ICs/Memory/Fundamentals_of_nonvolatile_memory
3.	https://link.springer.com/content/pdf/bbm%3A978-0-306-47972-4%2F1.pdf
4.	https://www.researchgate.net/publication/220649285_Memory_Fault_Modeling
5.	https://catalogimages.wiley.com/images/db/pdf/0471208132.excerpt.pdf

VLSI Design Laboratory -II
I M. Tech II Semester

Course Category	Professional Core	**Course Code**	19042L02
Course Type	Laboratory	**L-T-P-C**	4-0-0-2
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

The students are required to design and implement the Layout of the following Experiments of any SIX using CMOS 130nm Technology with Mentor Graphics Tool.

List of Experiments:

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Static RAM Cell.
6. Dynamic RAM Cell.
7. ROM
8. Digital-to-Analog-Converter.
9. Analog-to-Digital Converter.

PART-B: Mixed Signal Simulation

The students are required to perform the following experimental concepts with suitable complexity mixed-signal application based circuits of any FOUR (circuits consisting of both analog and digital parts) using necessary software tools.

1. List of experimental Concepts:
2. Analog circuit simulation.
3. Digital circuit simulation.
4. Mixed signal simulation.
5. Layout Extraction.
6. Parasitic values estimation from layout.
7. Layout Vs Schematic.
8. **Net List Extraction.**
9. **Design Rule Checks.**

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool, Mixed Signal simulator

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardwareKits

EMBEDDED SYSTEM DESIGN
I M. Tech III Semester

Course Category	Professional Core	**Course Code**	19043T07
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites		**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	List technologies, their integration, design flow and software development for Embedded systems	K3
CO2	Classify embedded processors, memory and its management, embedded input and output components, Bus integration and performance	K2
CO3	Summarize device drivers, Multitasking, process, i/o and file management; middleware and application software	K3
CO4	Explain Embedded system design and development, downloading and debugging	K3
CO5	Demonstrate Case studies like Power PC, Micro blaze, NIOS-II; design on Altera platform	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3				2							2
CO2	3				2							2
CO3	3				2							2
CO4	3	2		2	2							2
CO5	**3**	2		1	2							2

COURSE CONTENT	
UNIT I	**Introduction** An Embedded System-Definition, Examples, Current Technologies, Integration in system Design, Embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts
UNIT II	**Embedded Hardware** Embedded hardware building blocks, Embedded Processors – ISA architecture models, Internal processor design, processor performance, Board Memory – ROM, RAM, Auxiliary Memory, Memory Management of External Memory, Board Memory and performance. Embedded board Input / output – Serial versus Parallel I/O, interfacing the I/O components, I/O components and performance, Board buses – Bus arbitration and timing, Integrating the Bus with other board components, Bus performance
UNIT III	**Embedded Software** Device drivers, Device Drivers for interrupt-Handling, Memory device drivers, On-board bus device drivers, Board I/O drivers, Explanation about above drivers with suitable examples. Embedded operating systems – Multitasking and process Management, Memory Management, I/O and file system management, OS standards example – POSIX, OS performance guidelines, Board support packages, Middleware and Application Software –

	Middle ware, Middleware examples, Application layer software examples
UNIT IV	**Embedded System Design, Development, Implementation and Testing** Embedded system design and development lifecycle model, creating an embedded system architecture, introduction to embedded software development process and tools- Host and Target machines, linking and locating software, Getting embedded software into the target system, issues in Hardware-Software design and co-design. Implementing the design-The main software utility tool, CAD and the hardware, Translation tools, Debugging tools, testing on host machine, simulators, Laboratory tools, System Boot-Up.
UNIT V	Embedded System Design Case Studies Case studies Processor design approach of an embedded system– Power PC Processor based and Micro Blaze Processor based Embedded system design on Xilinx platform-NiosII Processor based Embedded system design on Altera platform Respective Processor architectures should be taken into consideration while designing an Embedded System

TEXT BOOKS	
1.	Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications,2005
2.	Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & SonsInc.2002.
REFERENCE BOOKS	
1.	Peter Marwedel, "Embedded System Design", Science Publishers,2007.
2.	Arnold S Burger, "Embedded System Design", CMP,2001
3.	Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition,2008
WEB RESOURCES	
1.	https://www.digimat.in/nptel/courses/video/106105159/L01.html
2.	https://www.coursera.org/learn/introduction-embedded-systems

TESTING AND TESTABILITY
I M. Tech III Semester

Course Category	Professional Core	**Course Code**	19043T08
Course Type	Theory	**L-T-P-C**	3-0-0-3
Prerequisites	Basic knowledge of testing and state machines	**Internal Assessment** **Semester End Examination** **Total Marks**	40 60 100

COURSE OUTCOMES		
Upon successful completion of the course, the student will be able to:		**Cognitive Level**
CO1	Remember the basic concepts of Analog and Digital testing devices used in chip designing	K3
CO2	Understand the concepts of simulation and design verification used in chip modeling	K2
CO3	Apply the concept of testing digital circuits used in industrial applications	K3
CO4	Analyze the build in self test testing procedures used in chip manufacturing	K3
CO5	Design TAP controllers used in testing process using BDSL	K3

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)												
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	2	3	1	2		3				2	1
CO2	2	1	3	1	2		1				2	2
CO3	2	2	3	2	1		2				2	3
CO4	2	2	3	1	2		1				2	2
CO5	2	2	3	1	1		3				2	2

COURSE CONTENT	
UNIT I	Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault
UNIT II	Logic and Fault Simulation : Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation
UNIT III	Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan
UNIT IV	Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per- Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST

UNIT V	Boundary Scan Standard : Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions

TEXT BOOKS	
1.	Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers
2.	
REFERENCE BOOKS	
1.	Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico PublishingHouse
2.	Digital Circuits Testing and Testability - P.K. Lala, AcademicPress
WEB RESOURCES	
1.	
2.	
3.	
4.	
5.	