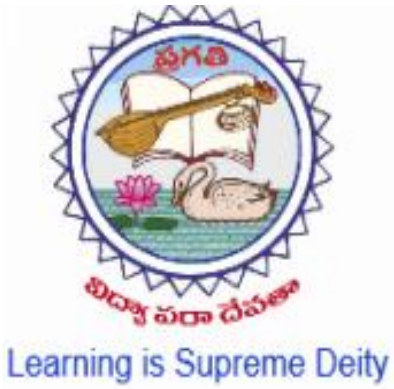
# COURSE STRUCTURE AND SYLLABUS

**For**

# M. Tech

# EMBEDDED SYSTEMS

*(Applicable for batches admitted from 2019-2020)*




# PRAGATI ENGINEERING COLLEGE

## (Autonomous)

Permanently Affiliated to JNT University Kakinada and Approved by AICTE, New Delhi,
Accredited by NAAC with "A" Grade
Recognized by UGC 2(f) and 12(b) under UGC act, 1956
1-378, ADB Road, Surampalem – 533 437, Near Peddapuram, E.G.Dist., A.P.

# PRAGATI ENGINEERING COLLEGE: SURAMPALEM

**(Autonomous)**

**EMBEDDED SYSTEMS**

## I Semester

| Sub Code | Name of the Subject | L | P | C |
|---|---|---|---|---|
| 19021T01 | Digital System Design | 4 | | 3 |
| 19021T02 | Embedded System Design | 4 | | 3 |
| 19021T03 | Embedded - C | 4 | | 3 |
| 19021D01<br>19021D02<br>19021D03 | **Elective I**<br>1. Sensors and Actuators<br>2. Network Security & Cryptography<br>3. Advanced Computer Architecture | 4 | | 3 |
| 19021D04<br>19021D05<br>19021D06 | **Elective II**<br>1. Embedded Computing<br>2. Soft Computing Techniques<br>3. Advanced Operating Systems | 4 | | 3 |
| 19021L01 | Laboratory<br>1. Embedded C-Laboratory | - | 3 | 2 |
| **Total** | | | | **17** |

## II Semester

| Sub Code | Name of the Subject | L | P | C |
|---|---|---|---|---|
| 19022T04 | Hardware Software Co-Design | 4 | | 3 |
| 19022T05 | Digital Signal Processors and Architecture | 4 | | 3 |
| 19022T06 | Embedded Networking | 4 | | 3 |
| 19022D07<br>19022D08<br>19022D09 | **Elective III**<br>1. CMOS Mixed Signal Circuit Design<br>2. Micro Electro Mechanical System Design<br>3. Internet Protocols | 4 | | 3 |
| 19022D10<br>19022D11<br>19022D12 | **Elective IV**<br>1. System on Chip Design<br>2. Wireless LANs and PANs<br>3. Multimedia and Signal Coding | 4 | | 3 |
| 19022L02 | Laboratory<br>1. Embedded Systems Design Laboratory | - | 3 | 2 |
| **Total** | | | | **17** |

# PRAGATI ENGINEERING COLLEGE: SURAMPALEM

**(Autonomous)**

## III Semester

| Sub Code | Name of the Subject | L | P | C |
|---|---|---|---|---|
| 19023T07 | Embedded Real Time Operating Systems | 4 | | 3 |
| 19023T08 | CPLD and FPGA Architectures and Applications | 4 | | 3 |
| 19023C01 | Comprehensive Viva-Voce | -- | -- | 3 |
| 19023S01 | Seminar – I | | | 2 |
| 19023P01 | Project Work Part – I | | | 6 |
| **Total** | | | | **17** |

## IV Semester

| Sub Code | Name of the Subject | L | P | C |
|---|---|---|---|---|
| 19024S02 | Seminar – II | | | 2 |
| 19024P02 | Project Work Part - II | | | 15 |
| **Total** | | | | **17** |

**The project will be evaluated at the end of the IV Semester**

**DIGITAL SYSTEM DESIGN**
**I M. Tech I Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19021T01 |
| **Course Type** | Theory | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | Analyse various Minimization Procedures for minimizing Switching functions and Camp Algorithms. | K3 |
| **CO2** | Design PLD's & PLA by using Minimization and Folding Algorithms | K3 |
| **CO3** | Design the Large-Scale Digital Systems | K3 |
| **CO4** | Analyse the Fault Diagnosis in Combinational Circuits. | K2 |
| **CO5** | Discuss the Fault Diagnosis in Sequential Circuits and its Experiments. | K2 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 3 | 3 | 3 | | | | | | | | | |
| **CO2** | 3 | 3 | 2 | | | | | | | | | |
| **CO3** | 3 | 3 | 1 | | | | | | | | | |
| **CO4** | 3 | 3 | 3 | | | | | | | | | |
| **CO5** | 3 | 3 | 2 | | | | | | | | | |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | Minimization Procedures and CAMP Algorithm: Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms. |
| **UNIT II** | PLA Design, Minimization and Folding Algorithms: Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples. |
| **UNIT III** | Design of Large Scale Digital Systems: Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs. |

| | |
|---|---|
| **UNIT IV** | Fault Diagnosis in Combinational Circuits: Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test. |
| **UNIT V** | Fault Diagnosis in Sequential Circuits: Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Logic Design Theory-N. N. Biswas, PHI,1993. |
| **2.** | Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001,TMH |
| **3.** | Digital system Design usingPLDd-Lala,2003 |
| **REFERENCE BOOKS** | |
| **1.** | Fundamentals of Logic Design – Charles H. Roth, 5th Ed., CengageLearning. |
| **2.** | Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & SonsInc,2003 |

**EMBEDDED SYSTEM DESIGN**
**I M. Tech I Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19021T02 |
| **Course Type** | Theory | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | ES | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | understand the basic concepts of digital signal processing | K3 |
| **CO2** | analyze the architectures for Programmable DSP Devices | K2 |
| **CO3** | understand Commercial Digital signal processing Devices and Programmable Digital Signal Processors | K3 |
| **CO4** | understand Analog Devices Family of DSP Devices Analog Devices Family of DSP Devices | K3 |
| **CO5** | analyze various interfacing devices. | K3 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 2 | 2 | 3 | | | | | | | | | |
| **CO2** | 2 | 3 | 3 | | | | | | | | | |
| **CO3** | 3 | 2 | 3 | | | | | | | | | |
| **CO4** | 3 | 2 | 3 | | | | | | | | | |
| **CO5** | 2 | 3 | 3 | | | | | | | | | |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Introduction** An Embedded System-Definition, Examples, Current Technologies, Integration in system Design, Embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts. |
| **UNIT II** | **Embedded Hardware** Embedded hardware building blocks, Embedded Processors – ISA architecture models, Internal processor design, processor performance, Board Memory – ROM, RAM, Auxiliary Memory, Memory Management of External Memory, Board Memory and performance.<br>Embedded board Input / output – Serial versus Parallel I/O, interfacing the I/O components, I/O components and performance, Board buses – Bus arbitration and timing, Integrating the Bus with other board components, Bus performance. |
| **UNIT III** | **Embedded Software** Device drivers, Device Drivers for interrupt-Handling, Memory device drivers, On-board bus device drivers, Board I/O drivers, Explanation about above drivers with suitable examples.<br>Embedded operating systems – Multitasking and process Management, Memory Management, I/O and file system management, OS standards example – POSIX, OS performance guidelines, Board support packages, Middleware and |

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|---|---|
| | Application Software – Middle ware, Middleware examples, Application layer software examples. |
| **UNIT IV** | **Embedded System Design, Development, Implementation and Testing** Embedded system design and development lifecycle model, creating an embedded system architecture, introduction to embedded software development process and tools- Host and Target machines, linking and locating software, Getting embedded software into the target system, issues in Hardware-Software design and co-design. Implementing the design-The main software utility tool, CAD and the hardware, Translation tools, Debugging tools, testing on host machine, simulators, Laboratory tools, System Boot-Up. |
| **UNIT V** | Embedded System Design Case Studies Case studies Processor design approach of an embedded system– Power PC Processor based and Micro Blaze Processor based Embedded system design on Xilinx platform-NiosII Processor based Embedded system design on Altera platform Respective Processor architectures should be taken into consideration while designing an Embedded System |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications, 2005. |
| **2.** | Frank Vahid, Tony D.Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002. |
| **REFERENCE BOOKS** | |
| **1.** | Peter Marwedel, "Embedded System Design", Science Publishers, 2007. |
| **2.** | Arnold S Burger, "Embedded System Design", CMP,2001. |
| **WEB RESOURCES** | |
| **1.** | https://youtu.be/zADj0k0waFY |
| **2.** | https://youtu.be/-eK_niCyf5Y |
| **3.** | https://youtu.be/PlavjNH_RRU |
| **4.** | https://youtu.be/MIPIMLZsuKU |
| **5.** | https://youtu.be/vd9ykB7fdmI |

**EMBEDDED C**
**I M. Tech I Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19021T03 |
| **Course Type** | Theory | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Basics of operating system | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | Able to understand Basics of operating system. | K3 |
| **CO2** | Able to unnderstand Basic concepts of Software Development Tools . | K2 |
| **CO3** | Able to understand module interfacing . | K3 |
| **CO4** | Able to understand Basics of network security . | K3 |
| **CO5** | Able to understand simulation and debugging tools. . | K3 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 2 | 3 | 2 | 2 | 2 | 1 | 0 | 0 | 1 | 2 | 1 | 1 |
| **CO2** | 2 | 2 | 2 | 3 | 2 | 2 | 0 | 0 | 1 | 2 | 1 | 1 |
| **CO3** | 3 | 3 | 2 | 2 | 3 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| **CO4** | 2 | 2 | 2 | 2 | 2 | 1 | 0 | 0 | 0 | 2 | 1 | 1 |
| **CO5** | **2** | 3 | 2 | 2 | 2 | 2 | 0 | 0 | 1 | 1 | 1 | 1 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Programming Embedded Systems in C**<br>Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions<br>**Introducing the 8051 Microcontroller Family**<br>Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions |
| **UNIT II** | **Reading Switches:** Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions |
| **UNIT III** | **Adding Structure to the Code** Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further |

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|---|---|
| | examples, Conclusions |
| **UNIT IV** | **Meeting Real-Time Constraints** Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions |
| **UNIT V** | **Case Study-Intruder Alarm System** Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008 |
| **REFERENCE BOOKS** | |
| **1.** | PICMCU C-An introduction to programming, The Microchip PIC in CCS C - Nigel Gardner. |
| **WEB RESOURCES** | |
| **1.** | **www.vssut.ac.in** |
| **2.** | **Searchsecurity.techtarget.com** |
| **3.** | **www.geeksforgeeks.com** |
| **4.** | **www.123seminarsonly.com** |
| **5.** | **www.slideshare.ne** |

**SENSORS AND ACTUATOR**
**I M. Tech I Semester**

| | | | |
|---|---|---|---|
| **Course Category** | ECE | **Course Code** | 19021D01 |
| **Course Type** | Theory (Elective I) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Sensors / Transducers:** Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization. Mechanical and Electromechanical Sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor – Types-Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors. |
| **UNIT II** | **Thermal Sensors:** Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermo sensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors – Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry –Heat Flux Sensors<br>**Magnetic sensors:** Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors – Anisotropic Magneto resistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors – Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros – Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors |
| **UNIT III** | **Radiation Sensors:** Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors. Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential - Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media . |
| **UNIT IV** | Smart Sensors: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The AutomationSensors-Applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring |
| **UNIT V** | Actuators Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Presure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection<br>Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors |

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|---|---|
| **TEXT BOOKS** | |
| **1.** | D. Patranabis – “Sensors and Transducers” – 2nd Ed.,PHI Learning Private Limited,2003. |
| **2.** | W. Bolton – “Mechatronics” –4th edition, Pearson Education Limited,2008 |
| **REFERENCE BOOKS** | |
| **1.** | Sensors And Actruators – D. Patranabis – 2nd Ed., PHI, 2013. |
| **WEB RESOURCES** | |

**NETWORK SECURITY & CRYPTOGRAPHY**
**I M. Tech I Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19021D02 |
| **Course Type** | Theory (Elective I) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Basics of Encryption techniques. | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | understand Classical Encryption Techniques. | K2 |
| **CO2** | Understand DES,RSA Algorithm | K2 |
| **CO3** | understand Discrete logorithms. | K2 |
| **CO4** | understand Hash and Mac Algorithm | K2 |
| **CO5** | understand Fire wall Design principles. | K2 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 2 | 3 | 2 | 2 | 2 | 1 | 0 | 0 | 1 | 2 | 1 | 1 |
| **CO2** | 2 | 2 | 2 | 3 | 2 | 2 | 0 | 0 | 1 | 2 | 1 | 1 |
| **CO3** | 3 | 3 | 2 | 2 | 3 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| **CO4** | 2 | 2 | 2 | 2 | 2 | 1 | 0 | 0 | 0 | 2 | 1 | 1 |
| **CO5** | **2** | 3 | 2 | 2 | 2 | 2 | 0 | 0 | 1 | 1 | 1 | 1 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | Introduction Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques |
| **UNIT II** | **Modern Techniques:** Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations. Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers. Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation. Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography. |
| **UNIT III** | **Number Theory:** Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms. Message authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs. |

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| **UNIT IV** | **Hash and Mac Algorithms**: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. Digital signatures and Authentication Protocols: Digital signatures, Authentication Protocols, Digital signature standards. Authentication Applications: Kerberos, X.509 directory Authentication service.Electronic Mail Security: Pretty Good Privacy, S/MIME. |
| **UNIT V** | IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management. Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction. Intruders, Viruses and Worms: Intruders, Viruses and Related threats. Fire Walls: Fire wall Design Principles, Trusted systems. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Cryptography and Network Security: Principles and Practice– William Stallings, 2000, PE. |
| **2.** | "Aplied Cryptography", Bruce Schneier, 2nd edition,Wley Publishers,2008. |
| **REFERENCE BOOKS** | |
| **1.** | Principles of Network and Systems Administration, Mark Burgess,John Wiey,2007. |
| **WEB RESOURCES** | |
| **1.** | **www.vssut.ac.in** |
| **2.** | **Searchsecurity.techtarget.com** |
| **3.** | **www.geeksforgeeks.com** |
| **4.** | **www.123seminarsonly.com** |
| **5.** | **www.slideshare.net** |

**ADVANCED COMPUTER ARCHITECTURE**
**I M. Tech I Semester**

| | | | |
|---|---|---|---|
| **Course Category** | ECE | **Course Code** | 19021D03 |
| **Course Type** | Theory (Elective I) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | Discuss the organisation of computer-based systems and how a range of design choices are influenced by applications | |
| **CO2** | Understand different processor architectures and system-level design processes. | |
| **CO3** | Understand the components and operation of a memory hierarchy and the range of performance issues influencing its design. | |
| **CO4** | Understand the organisation and operation of current generation parallel computer systems, including multiprocessor and multicore systems. | |
| **CO5** | Develop systems programming skills in the content of computer system design and organisation. | |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

**Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)**

| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 2 | 2 | 2 | 2 | 2 | 0 | 0 | 0 | 2 | 0 | 0 | 1 |
| **CO2** | 2 | 3 | 2 | 3 | 2 | 0 | 0 | 0 | 1 | 0 | 0 | 2 |
| **CO3** | 2 | 2 | 2 | 3 | 2 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| **CO4** | 2 | 3 | 2 | 2 | 3 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| **CO5** | **3** | 2 | 3 | 2 | 2 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Fundamentals of Computer Design:** Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, Measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, Classifying instruction set- MEmory addressing- type and size of operands, Operations in the instruction set. |
| **UNIT II** | **Pipelines:** Introduction, Basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design:Introduction, Review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory. |

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| **UNIT III** | **Instruction Level Parallelism the Hardware Approach:** Instruction Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation. ILP Software Approach Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software. |
| **UNIT IV** | **Multi Processors and Thread Level Parallelism:** Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization. |
| **UNIT V** | **Inter Connection and Networks:** Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier,2002. |
| **REFERENCE BOOKS** | |
| **1.** | John P. Shen and Miikko H. Lipasti - Modern Processor Design : Fundamentals of Super Scalar Processors,2013. |
| **2.** | Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill,1984. |
| **3.** | Advanced Computer Architecture - A Design Space Approach - Dezso Sima, Terence Fountain, Peter Kacsuk , Pearson Ed,1997 |
| **WEB RESOURCES** | |
| **1.** | |
| **2.** | |
| **3.** | |

**EMBEDDED COMPUTING**
**I M. Tech I Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19021D04 |
| **Course Type** | Theory(Elective II) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Basics of operating system | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | UnderstandBasics of operating system. | K2 |
| **CO2** | understand Basic concepts of Software Development Tools . | K2 |
| **CO3** | understand module interfacing . | K2 |
| **CO4** | understand Basics of network security . | K2 |
| **CO5** | understand simulation and debugging tools. . | K2 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 2 | 3 | 2 | 2 | 2 | 1 | 0 | 0 | 1 | 2 | 1 | 1 |
| **CO2** | 2 | 2 | 2 | 3 | 2 | 2 | 0 | 0 | 1 | 2 | 1 | 1 |
| **CO3** | 3 | 3 | 2 | 2 | 3 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| **CO4** | 2 | 2 | 2 | 2 | 2 | 1 | 0 | 0 | 0 | 2 | 1 | 1 |
| **CO5** | **2** | 3 | 2 | 2 | 2 | 2 | 0 | 0 | 1 | 1 | 1 | 1 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | Programming on Linux Platform:System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. Operating System Overview: Processes, Tasks, Threads, MultiThreading, Semaphore, Message Queue. |
| **UNIT II** | Introduction to Software Development Tools GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools. |
| **UNIT III** | Interfacing ModulesSensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing. |
| **UNIT IV** | Networking BasicsSockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security. |

| | |
|---|---|
| **UNIT V** | Intel Architecture 32-bit (IA32) Instruction Set Application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012 |
| **2.** | Linux Application Development - Michael K. Johnson, Erik W. Troan,Adission Wesley, 1998 |
| **3.** | Assembly Language for x86 Processors by Kip R. Irvine,7th edition Prentice-Hall publishers,2014 |
| **REFERENCE BOOKS** | |
| **1.** | Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne,wiley publisher, 8th edition,2008. |
| **2.** | Intel® 64 and IA-32 Architectures Software Developer Manuals. |
| **3.** | The Design of the UNIX Operating System by Maurice J. Bach PrenticeHall |
| **4.** | UNIX Network Programming by W. Richard Stevens |
| **WEB RESOURCES** | |
| **1.** | **www.vssut.ac.in** |
| **2.** | **Searchsecurity.techtarget.com** |
| **3.** | **www.geeksforgeeks.com** |
| **4.** | **www.123seminarsonly.com** |
| **5.** | **www.slideshare.net** |

**SOFT COMPUTING TECHNIQUES**
**I M. Tech I Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19021D05 |
| **Course Type** | Theory (Elective II) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Introduction:** Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems. |
| **UNIT II** | **Artificial Neural Networks:** Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller. |
| **UNIT III** | **Fuzzy Logic System:** Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system. |
| **UNIT IV** | **Genetic Algorithm:** Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and anD-colony search techniques for solving optimization problems. |
| **UNIT V** | **Applications:**GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999. |
| **2.** | Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994 |
| **REFERENCE BOOKS** | |
| **1.** | Fuzzy Sets, Uncertainty and Information - Klir G.J. &Folger T.A., Prentice-Hall of India Pvt. Ltd., 1993. |
| **2.** | Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994. |
| **3.** | Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers. |
| **4.** | Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi |
| **5.** | Elements of Artificial Neural Networks - KishanMehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International. |

| | |
|---|---|
| **6.** | Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education |
| **7.** | Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi. |
| **WEB RESOURCES** | |
| **1.** | |
| **2.** | |
| **3.** | |

**ADVANCED OPERATING SYSTEMS**
**I M. Tech I Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19021D06 |
| **Course Type** | Theory (Elective II) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Operating Systems | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | Understand the concepts of I/O function, Interrupts & Memory hierarchy in operating systems. | K2 |
| **CO2** | Interpret the concept of Unix & Linux in operating systems. | K4 |
| **CO3** | Perceive the concept of Pipes, FIFOs, Message queues & Semaphores. | K3 |
| **CO4** | Interpret the concept of ATM networks, Client - Server model, Remo procedure call and Group communication. | K4 |
| **CO5** | Perceive the concept of Clock synchronization, Bully algorithm, Ri algorithm, Dead lock in distributed systems. | K2 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 1 | 1 | 1 | 1 | 2 | 1 | | | | | | 2 |
| **CO2** | 1 | 1 | 1 | 1 | 2 | 1 | | | | | | 2 |
| **CO3** | 1 | 1 | 1 | 1 | 2 | 1 | | | | | | 2 |
| **CO4** | 1 | 1 | 1 | 1 | 2 | 1 | | | | | | 2 |
| **CO5** | 1 | 1 | 1 | 1 | 2 | 1 | | | | | | 2 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Introduction to Operating Systems:** Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System |
| **UNIT II** | **Introduction to UNIX and LINUX**: Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations |
| **UNIT III** | **System Calls:** System calls and related file structures, Input / Output, Process creation & termination. Inter Process Communication: Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI. |

| | |
|---|---|
| **UNIT IV** | **Introduction to Distributed Systems:** Goals of distributed system, Hardware and software concepts, Design issues. Communication in Distributed Systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication. |
| **UNIT V** | **Synchronization in Distributed Systems:** Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions Deadlocks :Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI. |
| **2.** | Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI |
| **3.** | The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill |
| **REFERENCE BOOKS** | |
| **1.** | Operating Systems: Internal and Design Principles -Stallings, 6th Ed., PE. |
| **2.** | Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE. |
| **3.** | Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley |
| **4.** | UNIX User Guide – Ritchie & Yates |
| **5.** | UNIX Network Programming - W.Richard Stevens, 1998, PHI |
| **WEB RESOURCES** | |
| **1.** | https://nptel.ac.in/courses/106106157/15 |
| **2.** | https://nptel.ac.in/courses/106106157/13 |
| **3.** | https://nptel.ac.in/courses/106106168 |

**EMBEDDED C LABORATORY**
**I M. Tech I Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19021L01 |
| **Course Type** | Laboratory | **L-T-P-C** | 4-0-0-2 |
| **Prerequisites** | EMBEDDED C PROGRAMMING | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | write the programs using C-Language according to the hardware requirements such as 8051/PIC Micro controllers or any ARM processor developerkits. | |
| **CO2** | Understand the experiment of the are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification | |
| **CO3** | develope for the implementation should be at the level of an embedded systemdesign | |
| **CO4** | gain the knowledge about Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOSLibrary, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER. (iv)LINUX Environment for the compilation using Eclipse IDE & Java withlatestversion. | |
| **CO5** | Gain the knowledge about the programs developed for the implementation should be at the level of an embedded systemdesign. | |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 3 | 3 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CO2** | 3 | 3 | 1 | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CO3** | 3 | 2 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CO4** | 2 | 2 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CO5** | **2** | 3 | 1 | 1 | 0 | 0 | 0 | 00 | 0 | 0 | 0 | 0 |

**List of Experiments:**

1. LED Blinking.
2. ASCII to Decimal vice versa conversion.
3. Basic Arithmetic operations.
4. PWM (Motor application).
5. Serial Communication (USART).
6. ADC and DAC implementation.
7. JTAG Debugger.
8. Seven segment display interfacing.
9. LCD display interfacing.
10. 3x4 keyboard interfacing.
11. Memory Device interfacing (Reading or Writing a file from external memory).
12. Temperature sensor/4 way Road control /Elevator.

**Lab Requirements:**

**Software:**

1. Keil Micro-vision IDE or Eclipse IDE for C and C++ (YAGARTO Eclipse IDE)
2. LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

**Hardware:**

**1**. Thedevelopment kits of 8051/PIC Micro controllers or any ARM processor.

**HARDWARE SOFTWARE CO-DESIGN**
**I M. Tech II Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19022T04 |
| **Course Type** | Theory | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | acquire the knowledge about system specification and modeling. | K2 |
| **CO2** | learn the formulation of partitioning the hardware and software | K2 |
| **CO3** | analyze about the hardware and software integration | K2 |
| **CO4** | study the hardware design languages and its components | K2 |
| **CO5** | formulate the design specification and module creation | K2 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 3 | 2 | 1 | 1 | | | | | | | | |
| **CO2** | 3 | 2 | 2 | 1 | | | | | | | | |
| **CO3** | 3 | 3 | 2 | 1 | | | | | | | | |
| **CO4** | 3 | 2 | 1 | 1 | | | | | | | | |
| **CO5** | 3 | 3 | 3 | 1 | | | | | | | | |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Co- Design Issues:** Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.<br>Co- Synthesis Algorithms:Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis. |
| **UNIT II** | **Prototyping and Emulation:** Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure<br>Target Architectures:Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems. |
| **UNIT III** | Compilation Techniques and Tools for Embedded Processor Architectures:Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment. |
| **UNIT IV** | Design Specification and Verification: Design, co-design, the codesign computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification. |

| | |
|---|---|
| **UNIT V** | Languages for System – Level Specification and Design-I: Systemlevel specification, design representation for system level synthesis, system level specification languages.<br>Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Hardware / Software Co- Design Principles and Practice – JorgenStaunstrup, Wayne Wolf – 2009, Springer. |
| **2.** | Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers. |
| **REFERENCE BOOKS** | |
| **1.** | A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer Publications. |
| **WEB RESOURCES** | |

**DIGITAL SIGNAL PROCESSORS & ARCHITECTURS**
**I M. Tech II Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19022T05 |
| **Course Type** | Theory | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | DSP | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | understand the basic concepts of digital signal processing | K2 |
| **CO2** | analyze the architectures for Programmable DSP Devices | K4 |
| **CO3** | understand Commercial Digital signal processing Devices and Programmable Digital Signal Processors | K2 |
| **CO4** | understand Analog Devices Family of DSP Devices Analog Devices Family of DSP Devices | K2 |
| **CO5** | analyze various interfacing devices. | K4 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 3 | 3 | 3 | | | | | | | | | |
| **CO2** | 2 | 3 | 3 | | | | | | | | | |
| **CO3** | 3 | 3 | 3 | | | | | | | | | |
| **CO4** | 3 | 2 | 2 | | | | | | | | | |
| **CO5** | 2 | 3 | 2 | | | | | | | | | |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | Introduction to Digital Signal Processing Introduction, a Digital signal processing system, the sampling process, discrete time sequences.<br>Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time- invariant systems, Digital filters, Decimation and interpolation. Computational Accuracy in DSP Implementations Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter. |
| **UNIT II** | Architectures for Programmable DSP Devices Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing. |
| **UNIT III** | Programmable Digital Signal Processors Commercial Digital signal processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors. |

| | |
|---|---|
| **UNIT IV** | Analog Devices Family of DSP Devices Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP- 2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals. |
| **UNIT V** | Interfacing Memory and I/O Peripherals to Programmable DSP Devices Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004. |
| **2.** | A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009 |
| **3.** | Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007 |
| **REFERENCE BOOKS** | |
| **1.** | Digital Signal Processors, Architecture, Programming and ApplicationsB. Venkataramani and M. Bhaskar, 2002, TMH. |
| **2.** | DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co. |
| **3.** | Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI |
| **4.** | The Scientist and Engineer‟s Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997 |
| **WEB RESOURCES** | |
| **1.** | https://www.youtube.com/watch?v=6dFnpz_AEyA&list=RDQMVTlXem6siiM&start_radio=1 |
| **2.** | https://www.youtube.com/watch?v=rTbochn9s2w |
| **3.** | https://www.youtube.com/watch?v=D-TM91xLZY4 |

**EMBEDDED NETWORKING**
**I M. Tech II Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19022T06 |
| **Course Type** | Theory | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Microcontroller and microprocessors, Computer Networks | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | Understand various communication protocols and port programming | K2 |
| **CO2** | Compute program to interface PIC microcontroller and CAN bus and USB | K2 |
| **CO3** | Build a network using Ethernet cables and controllers | K3 |
| **CO4** | Analyze Serving web pages that respond to user Input and Keeping Devices and Networksecure | K4 |
| **CO5** | Apply MAC protocols and topologies using wireless sensor networks | K3 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | **CO1** | 2 | 1 | 2 | 1 | 2 | - | - | - | - | - | - |
| **CO2** | **CO2** | 1 | 2 | 1 | 2 | 2 | - | - | - | - | - | - |
| **CO3** | **CO3** | 2 | 1 | 3 | 1 | 1 | - | - | - | - | - | - |
| **CO4** | **CO4** | 2 | 2 | 1 | 1 | 1 | - | - | - | - | - | - |
| **CO5** | **CO5** | 2 | 1 | 2 | 2 | 1 | - | - | - | - | - | - |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Embedded Communication Protocols:** Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Fire wire. |
| **UNIT II** | **USB and CAN Bus:** USB bus-Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN. |
| **UNIT III** | **Ethernet Basics:** Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol. |
| **UNIT IV** | **Embedded Ethernet:** Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure |

| | |
|---|---|
| UNIT V | **Wireless Embedded Networking:** Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing |

| | |
|---|---|
| **TEXT BOOKS** | |
| **1.** | Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002. |
| **2.** | Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port -Jan Axelson, Penram Publications, 1996 |
| **REFERENCE BOOKS** | |
| **1.** | Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier2008 |
| **2.** | Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications,2003 |
| **3.** | Networking Wireless Sensors - Bhaskar KrishnamachariÀÛÜ, Cambridge press2005 |
| **WEB RESOURCES** | |
| **1.** | https://www.highintegritysystems.com/rtos/rtos-training-videos/ |

**CMOS MIXED SIGNAL CIRCUIT DESIGN**
**I M. Tech II Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19022D07 |
| **Course Type** | Theory (Elective III) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters. |
| **UNIT II** | Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications |
| **UNIT III** | Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters |
| **UNIT IV** | Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time interleaved converters. |
| **UNIT V** | Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002 |
| **2.** | CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010. |
| **3.** | Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013 |
| **REFERENCE BOOKS** | |
| **1.** | CMOS Integrated Analog-to- Digital and Digital-to-Analog convertersRudy Van De Plassche, Kluwer Academic Publishers, 2003 |
| **2.** | Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005. |
| **3.** | CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009. |
| **WEB RESOURCES** | |

**MICRO ELECTRO MECHANICAL SYSTEM DESIGN**
**I M. Tech II Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19022D08 |
| **Course Type** | Theory (Elective III) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Basics of Mechanical parts and electronic circuits. | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | understand Basic structures of MEM Devices | K2 |
| **CO2** | find Transient Response of the MEMS | K2 |
| **CO3** | Understand Two terminal MEM Structure. | K2 |
| **CO4** | study the applications of MEMS. | K2 |
| **CO5** | study the MEMS process flow. | K2 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 2 | 3 | 2 | 2 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| **CO2** | 2 | 3 | 2 | 2 | 2 | 0 | 0 | 0 | 1 | 0 | 0 | 2 |
| **CO3** | 3 | 2 | 3 | 2 | 2 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| **CO4** | 2 | 2 | 2 | 2 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| **CO5** | **3** | 2 | 2 | 2 | 2 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | Introduction Basic structures of MEM devices – (Canti-Levers, Fixed Beams diaphragms). Broad Response of Micro electromechanical systems (MEMS) to Mechanical (Force, pressure etc.) Thermal, Electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc. |
| **UNIT II** | Review of mechanical concepts like stress, strain, bending moment, deflection curve. Differential equations describing the deflection under concentrated force, Distributed force, distributed force, Deflection curves for cantilevers fixed beam. Electrostatic excitation – columbic force between the fixed and moving electrodes. Deflection with voltage in C.L, Deflection Vs Voltage curve, critical fringe field – field calculations using Laplace equation. Discussion on the approximate solutions – Transient response of the MEMS. |
| **UNIT III** | Types Two terminal MEMS - capacitance Vs voltage Curve – Variable capacitor. Applications of variable capacitors. Two terminal MEM structures. Three terminal MEM structures – Controlled variable capacitors – MEM as a switch and possible applications |
| **UNIT IV** | MEM Circuits & Structures MEM circuits & structures for simple GATES- AND, OR, NAND, NOR, Exclusive OR, simple MEM configurations for flip-flops triggering |

| | |
|---|---|
| | applications to counters, converters. Applications for analog circuits like frequency converters, wave shaping. RF Switches for modulation. MEM Transducers for pressure, force temperature. Optical MEMS |
| **UNIT V** | MEM Technologies Silicon based MEMS- Process flow – Brief account of various processes and layers like fixed layer, moving layers spacers etc., and etching technologies. Metal Based MEMS: Thin and thick film technologies for MEMS. Process flow and description of the processes, Status of MEMS in the current electronics scenario. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | MEMS Theory, Design and Technology - GABRIEL. M.Review, R.F.,2003, John wiley & Sons. . |
| **2.** | Strength of Materials –Thimo Shenko, 2000, CBS publishers & Distributors. |
| **3.** | MEMS and NEMS, Systems Devices; and Structures – Servey E.Lyshevski, 2002, CRC ss |
| **REFERENCE BOOKS** | |
| **1.** | Sensor Technology and Devices - Ristic L. (Ed) , 1994, Artech House, London. |
| **WEB RESOURCES** | |
| **1.** | www.mems -exchange.org |
| **2.** | www.lboro.ac.uk |
| **3.** | www.all about circuits.com |
| **4.** | www.Engineeringproductdesign.com |
| **5.** | www.sciencedirect.com |

**INTERNET PROTOCOLS**
**I M. Tech II Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19022D09 |
| **Course Type** | Theory (Elective III) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Basics of internet protocols | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | Independently understand basic computer network technology | K2 |
| **CO2** | Understand and explain Data Communications System and its components | K2 |
| **CO3** | Identify the different types of network devices and their functions within a network | K3 |
| **CO4** | Understand and building the skills of subnetting and routing mechanisms. | K2 |
| **CO5** | Familiarity with the basic protocols of network security , and how they can be used to assist in network design and implementation. | K2 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

**Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)**

| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 2 | 2 | 2 | 2 | 2 | 0 | 0 | 0 | 2 | 0 | 0 | 1 |
| **CO2** | 2 | 3 | 2 | 3 | 2 | 0 | 0 | 0 | 1 | 0 | 0 | 2 |
| **CO3** | 3 | 2 | 3 | 3 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| **CO4** | 2 | 3 | 2 | 2 | 2 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| **CO5** | **2** | 2 | 3 | 2 | 2 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Internetworking Concepts:**Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level Interconnection, Properties of thee Internet, Internet Architecture, Wired LANS, Wireless LANs, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite.<br>**IP Address: Classful Addressing:**Introduction, Classful Addressing, Other Issues, Sub-netting and Super-netting Classless Addressing: Variable length Blocks, Sub-netting, Address Allocation. Delivery, Forwarding, and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router.ARP and RARP:ARP, ARP Package, RARP. |
| **UNIT II** | **Internet Protocol (IP):**Datagram, Fragmentation, Options, Checksum, IP V.6.Transmission Control Protocol (TCP):TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times.Stream Control Transmission Protocol (SCTP):SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control. Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.<br>**Classical TCP Improvements:**Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP |

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|---|---|
| **UNIT III** | Unicast Routing Protocols (RIP, OSPF, and BGP): Intra and Interdomain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.<br>Multicasting and Multicast Routing Protocols:Unicast - MulticastBroadcast, Multicast Applications, Multicast Routing, Multicast Link<br>State Routing: MOSPF, Multicast Distance Vector: DVMRP. |
| **UNIT IV** | Domain Name System (DNS): Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet.<br>Remote Login TELNET:Concept, Network Virtual Terminal (NVT). File Transfer FTP and TFTP: File Transfer Protocol (FTP). Electronic Mail:SMTP and POP.<br>Network Management-SNMP:Concept, Management Components, World Wide Web- HTTP Architecture. |
| **UNIT V** | **Multimedia:** Digitizing Audio and Video, Network security, security in the internet firewalls. Audio and Video Compression, Streaming Stored Audio/Video, Streaming Live udio/Video, Real-Time Interactive Audio/ Video, RTP, RTCP, Voice Over IP. Network Security, Security in the Internet, Firewalls. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | TCP/IP Protocol Suite- Behrouz A. Forouzan, Third Edition, TMH,2005. |
| **2.** | Internetworking with TCP/IP- Comer, 6th edition, PHI,2013. |
| **REFERENCE BOOKS** | |
| **1.** | High performance TCP/IP Networking- Mahbub Hassan, Raj Jain, PHI, 2005 |
| **2.** | Data Communications & Networking – B.A. Forouzan – 2 nd Edition – TMH,2000. |
| **3.** | High Speed Networks and Internets- William Stallings, Pearson Education, 2002. |
| **4.** | Data and Computer Communications, William Stallings, 7th Edition., PEI. |
| **5.** | The Internet and Its Protocols – Adrin Farrel, Elsevier, 2005. |
| **WEB RESOURCES** | |
| **1.** | http://www.tcpipguide.com/free/index.htm |

**SYSTEM ON CHIP DESIGN**
**I M. Tech II Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19022D10 |
| **Course Type** | Theory (Elective IV) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Basics of chip design | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | Able to understand System Architecture. | |
| **CO2** | Able to understand Basic concepts in Processor Architecture. | |
| **CO3** | Able to understand SOC Memory System. | |
| **CO4** | Able to understand Customization and Configuration. | |
| **CO5** | Able to understand Design and evaluation . | |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

**Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)**

| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 2 | 3 | 2 | 2 | 2 | 1 | 0 | 0 | 1 | 2 | 1 | 1 |
| **CO2** | 2 | 2 | 2 | 3 | 2 | 2 | 0 | 0 | 1 | 2 | 1 | 1 |
| **CO3** | 3 | 3 | 2 | 2 | 3 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| **CO4** | 2 | 2 | 2 | 2 | 2 | 1 | 0 | 0 | 0 | 2 | 1 | 1 |
| **CO5** | **2** | 3 | 2 | 2 | 2 | 2 | 0 | 0 | 1 | 1 | 1 | 1 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity. |
| **UNIT II** | Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors. |
| **UNIT III** | Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction. |
| **UNIT IV** | Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing |

| | |
|---|---|
| | Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism |
| **UNIT V** | Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression. |

| | |
|---|---|
| **TEXT BOOKS** | |
| **1.** | Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiley India Pvt. Ltd,2011. |
| **2.** | ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional |
| **REFERENCE BOOKS** | |
| **1.** | Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer |
| **2.** | Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM |
| **3.** | System on Chip Verification – Methodologies and Techniques – Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers. |
| **WEB RESOURCES** | |
| **1.** | **www.vssut.ac.in** |
| **2.** | **Searchsecurity.techtarget.com** |
| **3.** | **www.geeksforgeeks.com** |
| **4.** | **www.123seminarsonly.com** |
| **5.** | **www.slideshare.net** |

**WIRELESS LANs AND PANs**
**I M. Tech II Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19022D11 |
| **Course Type** | Theory (Elective IV) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Antennas and propagation, cellular and mobile communications. | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | Understand the basics of wireless system and protocols | |
| **CO2** | understand the concepts of wireless lan and various technology | |
| **CO3** | Understand the basics of IEEE standards for Wireless Lans | |
| **CO4** | understand the concepts of PANs and Bluetooth technology | |
| **CO5** | Know the concept of IEEE standards for PAN | |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

**Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)**

| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CO1** | 2 | 1 | 1 | -- | -- | - | - | - | - | - | - | - |
| **CO2** | 2 | 1 | 1 | -- | -- | - | 1 | - | - | - | - | - |
| **CO3** | 1 | 2 | 2 | -- | -- | - | - | - | - | - | - | - |
| **CO4** | 3 | 2 | 1 | -- | -- | - | - | - | - | - | - | - |
| **CO5** | **1** | 2 | 1 | -- | -- | - | - | - | - | - | - | - |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Wireless System & Random Access Protocols:**Introduction, First and Second Generation Cellular Systems, Cellular Communications from 1G to 3G, Wireless 4G systems, The Wireless Spectrum; Random Access Methods: Pure ALOHA, Slotted ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA). |
| **UNIT II** | **Wireless LANs:** Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology |
| **UNIT III** | **The IEEE 802.11 Standard for Wireless LANs:** Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.11e MAC protocol |
| **UNIT IV** | **Wireless PANs:** Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, |

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|---|---|
| | Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assigment, Scatternet formation. |
| **UNIT V** | **The IEEE 802.15 working Group for WPANs:** The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband. |

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|---|---|
| **TEXT BOOKS** | |
| **1.** | Ad Hoc and Sensor Networks, Carlos de MoraisCordeiro and DharmaPrakashAgrawal, WorldsScientific,2011 |
| **2.** | Wireless Communications and Networking, Vijay K.Garg, Morgan Kaufmann Publishers,2009 |
| **REFERENCE BOOKS** | |
| **1.** | Wireless Networks-KavehPahlaram, Prashant Krishnamurthy, PHI,2002 |
| **2.** | Wireless Communication- Marks Ciampor, JeorgeOlenewa, Cengage Learning, 2007. |
| **WEB RESOURCES** | |
| **1.** | https://www.youtube.com/watch?v=wix1mX1X__M |
| **2.** | https://www.diffen.com/difference/LAN_vs_WAN |
| **3.** | https://slideplayer.com/slide/8125949/ |
| **4.** | https://www.youtube.com/watch?v=qGnzKp263bs |
| **5.** | https://www.youtube.com/watch?v=yOiqxgJMr2M |

**MULTIMEDIA AND SIGNAL CODING**
**I M. Tech II Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19022D12 |
| **Course Type** | Theory(Elective IV) | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Signals & Systems | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | Interpret the key concepts of image and video color patterns in Multimedia. | |
| **CO2** | Illustrate different types of Video Signals, Analog Video & Digital Video formats. | |
| **CO3** | Interpret the concepts of different Compression Algorithms like Lossless & Lossy Compression<br>Techniques in image processing. | |
| **CO4** | Develop basic algorithms in Video Compression like Quantization, Encoder and Decoder and MPEG1<br>And MPEG2. | |
| **CO5** | Perceive the concepts ofAudio Compression Techniques like Linear Predictive Coding, MPEG Audio Compression Algorithms. | |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 1 | 2 | 1 | 1 | 2 | | | | | | | 2 |
| **CO2** | 3 | 3 | 1 | 1 | 3 | | | | | | | 3 |
| **CO3** | 3 | 3 | 1 | 3 | 3 | | | | | | | 3 |
| **CO4** | 2 | 3 | 1 | 3 | 2 | | | | | | | 3 |
| **CO5** | 3 | 3 | 1 | 3 | 2 | | | | | | | 3 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | **Introduction to Multimedia:** Multimedia, World Wide Web, Overview of Multimedia Tools, Multimedia Authoring, Graphics/ Image Data Types, and File Formats.<br>**Color in Image and Video:** Color Science – Image Formation, Camera Systems, Gamma Correction, Color Matching Functions, CIE Chromaticity Diagram, Color Monitor Specifications, Outof- Gamut Colors, White Point Correction, XYZ to RGB Transform, Transform with Gamma Correction, LAB Color Model. Color Models in Images – RGB Color Model for CRT Displays, Subtractive Color: CMY Color Model, Transformation from RGB to CMY, Under Color Removal: CMYK System, Printer Gamuts, Color Models in Video – Video Color Transforms, YUV Color Model, YIQ Color Model, Ycbcr Color Model. |
| **UNIT II** | **Video Concepts:** Types of Video Signals, Analog Video, Digital Video.<br>**Audio Concepts:** Digitization of Sound, Quantization and Transmission of Audio. |

| | |
|---|---|
| **UNIT III** | **Compression Algorithms:** Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.<br>**Lossy Image Compression Algorithms:** Transform Coding: KLT And DCT Coding, Wavelet Based Coding.<br>Image Compression Standards: JPEG and JPEG2000. |
| **UNIT IV** | **Video Compression Techniques:** Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2. |
| **UNIT V** | **Audio Compression Techniques:** ADPCM in Speech Coding, G.726 ADPCM, Vocoders – Phase Insensitivity, Channel Vocoder, Formant Vocoder, Linear Predictive Coding, CELP, Hybrid Excitation, Vocoders, MPEG Audio – MPEG Layers, MPEG Audio Strategy, MPEG Audio Compression Algorithms, MPEG-2 AAC, MPEG-4 Audio. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Fundamentals of Multimedia – Ze- Nian Li, Mark S. Drew, PHI,2010. |
| **2.** | MultimediaSignals&Systems–MrinalKr. MandalSpringerInternational |
| **REFERENCE BOOKS** | |
| **1.** | Multimedia Communication Systems – Techniques, Stds& Netwroks K.R. Rao,Zorans. Bojkoric, Dragorad A.Milovanovic, 1st Edition,2002 |
| **2.** | Fundamentals of Multimedia Ze- Nian Li, Mark S.Drew, Pearson Education (LPE), 1st Edition,2009 |
| **3.** | Multimedia Systems John F. Koegel Bufond Pearson Education (LPE), 1st Edition,2003. |
| **4.** | Digital Video Processing – A. Murat Tekalp, PHI,1996 |
| **5.** | Video Processing and Communications – Yaowang, Jorn Ostermann, Ya-QinZhang, Pearson, 2002. |
| **WEB RESOURCES** | |
| **1.** | https://nptel.ac.in/courses/117105081/3 |
| **2.** | https://slideplayer.com/slide/8060552/ |

**Embedded System Design Laboratory**
**I M. Tech II Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19022L02 |
| **Course Type** | Laboratory | **L-T-P-C** | 4-0-0-2 |
| **Prerequisites** | **ARM-926 with PERFECT RTOS And** ARM-CORTEX processor using any open source RTOS | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | To understand to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits andARM-Cortex. | |
| **CO2** | To develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification | |
| **CO3** | The programs developed for the implementation should be at the level of an embedded systemdesign. | |
| **CO4** | Implement the interfacing of display with the ARM- CORTEXprocessor. | |
| **CO5** | Different design platforms used for an embedded systems applications | |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 3 | 3 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CO2** | 3 | 2 | 1 | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CO3** | 3 | 2 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CO4** | 3 | 2 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CO5** | 3 | 3 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Course Content:**

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.
9. Implement the interfacing of display with the ARM- CORTEX processor.
10. Interface ADC and DAC ports with the Input and Output sensitive devices.
11. Simulate the temperature DATA Logger with the SERIAL communication with PC.
12. Implement the developer board as a modem for data communication using serial port communication between two PC's.

**EMBEDDED AND REAL TIME OPERATING SYSTEM**
**I M. Tech III Semester**

| | | | |
|---|---|---|---|
| **Course Category** | ECE | **Course Code** | 19023T07 |
| **Course Type** | Theory | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | Microprocessors & Microcontrollers | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | Know about the fundamentals of operating systems and their importance in real time applications | K3 |
| **CO2** | Apply programming concepts of real-time operating system designed and their importance in embedded system design. | K2 |
| **CO3** | Analyze case studies of embedded system design and perform coding for different applications | K3 |
| **CO4** | Understand target image creation in Windows XP operating system and Linux OS | K3 |
| **CO5** | Develop a programming in RT Linux semaphore management, Mutex | K3 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 2 | 1 | 1 | 1 | 3 | - | - | - | - | - | - | 1 |
| **CO2** | 1 | 2 | 1 | 2 | 2 | - | - | - | - | - | - | - |
| **CO3** | 3 | 2 | 3 | 1 | 1 | - | - | - | - | - | - | 1 |
| **CO4** | 2 | 2 | 1 | 1 | 1 | - | - | - | - | - | - | - |
| **CO5** | 2 | 2 | 2 | 1 | 1 | - | - | - | - | - | - | - |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | Introduction OS Services, Process Management, Timer Functions, Event Functions, Memory Management, Device, File and IO Systems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls, Real-Time Operating Systems, Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latency and Response of the Tasks as Performance Metrics, OS Security. |
| **UNIT II** | RTOS Programming Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS-II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS OSEK, RTOS Linux 2.6.x and RTOS RT Linux. |
| **UNIT III** | Program Modeling – Case Studies Case study of embedded system design and coding for an Automatic Chocolate Vending Machine (ACVM) Using Mucos RTOS, case study of digital camera hardware and software architecture, case study of coding for sending application layer byte streams on a TCP/IP Network Using RTOS Vx Works, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs. |

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|---|---|
| **UNIT IV** | Target Image Creation & Programming in Linux Off-The-Shelf Operating Systems, Operating System Software, Target Image Creation for Window XP Embedded, Porting RTOS on a Micro Controller based Development Board.<br>Overview and programming concepts of Unix/Linux Programming, Shell Programming, System Programming. |
| **UNIT V** | Programming in RT Linux Overview of RT Linux, Core RT Linux API, Program to display a message periodically, semaphore management, Mutex, Management, Case Study of Appliance Control by RT Linux System. |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Dr. K.V.K.K. Prasad: "Embedded/Real-Time Systems" Dream Tech Publications, Black pad book,2003. |
| **2.** | Rajkamal: "Embedded Systems-Architecture, Programming and Design", Tata McGraw Hill Publications, Second Edition, 2008. |
| **REFERENCE BOOKS** | |
| **1.** | Labrosse, "Embedding system building blocks ", CMP publishers,1999. |
| **2.** | Rob Williams," Real time Systems Development", Butterworth Heinemann Publications,2005. |
| **WEB RESOURCES** | |
| **1.** | http://www.unicoi.com/product_suite_pages/fusion_networking_product_suite.htm |

**CPLD AND FPGA ARCHITECURES AND APPLICATIONS**
**I M. Tech III Semester**

| | | | |
|---|---|---|---|
| **Course Category** | Professional Core | **Course Code** | 19023T08 |
| **Course Type** | Theory | **L-T-P-C** | 3-0-0-3 |
| **Prerequisites** | | **Internal Assessment**<br>**Semester End Examination**<br>**Total Marks** | 40<br>60<br>100 |

| **COURSE OUTCOMES** | | |
|---|---|---|
| **Upon successful completion of the course, the student will be able to:** | | **Cognitive Level** |
| **CO1** | understand various architectures and device technologies of PLD's | K2 |
| **CO2** | discuss the architectures and applications of FPGA Programming Technologies | K2 |
| **CO3** | understand various architectures and programming technologies of SRAM Programmable FPGAs | K2 |
| **CO4** | Discuss various architectures and programming technologies of Anti-Fuse Programmed FPGAs | K2 |
| **CO5** | design examples of various CPLD and FPGA Applications and to discuss the General Design Issues | K3 |

K1: Remember, K2: Understand, K3: Apply, K4: Analyze, K5: Evaluate, K6: Create.

| **Contribution of Course Outcomes towards achievement of Program Outcomes (1 – Low, 2 - Medium, 3 – High)** | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** |
| **CO1** | 3 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **CO2** | 3 | 2 | 2 | 2 | 2 | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| **CO3** | 3 | 2 | 2 | 2 | 2 | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| **CO4** | 3 | 2 | 2 | 2 | 2 | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| **CO5** | **3** | 3 | 3 | 3 | 3 | 0 | 0 | 0 | 0 | 0 | 3 | 0 |

| **COURSE CONTENT** | |
|---|---|
| **UNIT I** | Introduction to Programmable Logic Devices Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation**.** |
| **UNIT II** | Field Programmable Gate Arrays Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs. |
| **UNIT III** | SRAM Programmable FPGAs Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures. |
| **UNIT IV** | Anti-Fuse Programmed FPGAsIntroduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures |

| | |
|---|---|
| **UNIT V** | Design Applications General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture |

| **TEXT BOOKS** | |
|---|---|
| **1.** | Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition,1994. |
| **2.** | Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John,2nd Ed., Cengage Learning,1998. |
| **REFERENCE BOOKS** | |
| **1.** | Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India,1995. |
| **2.** | Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/ Samiha Mourad, Pearson Low Price Edition,1994. |
| **3.** | Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier Newnes,2008. |
| **4.** | FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series,2004. |
| **WEB RESOURCES** | |
| **1.** | https://nptel.ac.in/courses/...contents/IIT%20Kharagpur/.../Pdf/Lesson-20.p... |
| **2.** | https://nptel.ac.in/courses/117108040/35 |
| **3.** | https://nptel.ac.in/.../Field%20Programmable%20Gate%20Arrays%20 |
| **4.** | pldworld.org/html/technote/intro.cpld.fpga.design.pdf |