COURSE STRUCTURE AND SYLLABUS

For

M.Tech

VLSI SYSTEM DESIGN

(*Applicable for batches admitted from 2016-17*)

PRAGATI ENGINEERING COLLEGE

(AUTONOMOUS)

Permanently Affiliated to JNTUK, Kakinada, Accredited by NAAC with "A" Grade
Recognized by UGC 2(f) and 12(b) under UGC act, 1956
1-378, ADB Road, Surampalem – 533 437
Near Peddapuram, E.G.Dist, Andhra Pradesh

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I Semester

S.No.	Subject Code	Subject	L	P	C
1	16041T01	VLSI Design Automation	4		3
2	16041T02	CMOS Analog IC Design	4		3
3	16041T03	CPLD and FPGA Architectures and Applications	4		3
4	16041T04	CMOS Digital IC Design	4		3
5	**Elective I**		4	-	3
	16041D01	1. ASIC Design			
	16041D02	2. Advanced Operating Systems			
	16041D03	3. Soft Computing Techniques			
6	**Elective II**		4	-	3
	16041D04	1. Digital Design using HDL			
	16041D05	2. Advanced Computer Architecture			
	16041D06	3. Hardware Software Co-Design			
7	16041L01	VLSI Laboratory-I	-	3	2
Total Credits					**20**

II Semester

S.No.	Subject Code	Subject	L	P	C
1	16042T05	Low Power VLSI Design	4	-	3
2	16042T06	CMOS Mixed Signal Circuit Design	4	-	3
3	16042T07	ReconfigurableArchitecturesFor VLSI	4	-	3
4	16042T08	Design For Testability	4	-	3
5	**Elective III**		4	-	3
	16042D07	1. Scripting Languages			
	16042D08	2. Digital Signal Processors & Architectures			
	16042D09	3. VLSI Signal Processing			
6	**Elective IV**		4	-	3
	16042D10	1 High Speed VLSI			
	16042D11	2 Optimization Techniques in VLSI Design			
	16042D12	3 Semiconductor Memory Design and Testing			
7	16042L02	VLSI Laboratory-II	-	3	2
Total Credits					**20**

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III Semester

S.No.	Subject Code	Subject	L	P	C
1	16043P01	Seminar -I	-	-	2
2	--	Project Work Part-I	-	-	18
Total Credits			-	-	**20**

IV Semester

S.No.	Subject Code	Subject	L	P	C
1	16044P03	Seminar - II	-	-	2
2	16043P02	Project Work Part-II	-	-	18
Total Credits			-	-	**20**

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VLSI DESIGN AUTOMATION

UNIT I - DATA STRUCTURES AND BASIC ALGORITHMS

Basic terminology – Complexity Issues and NP-Hardness: algorithms for NPhard problems-Basic algorithms: Graph algorithms, computational Geometry algorithms- Basic data structures-Graph algorithms for physical design: classes of graphs in physical design, relationship between graph classes, 11 graph problems in physical design, algorithms for Interval graphs, permutation graphs and circle graphs.

UNIT II - PARTITIONING AND CLUSTERING

Partitioning and Clustering Metrics -Move-Based Partitioning Methods - Mathematical Partitioning Formulations -Clustering :Hierarchical Clustering ,Agglomerative Clustering -Multilevel Partitioning.

UNIT III - FLOORPLANNING AND PLACEMENT

Floorplanning: Early research-Silicing floorplan - Floorplan representationPackaging floorplan epresentation-Recent advances in floorplanning. Placement-Introduction- Problem formulation- Simulation based placement algorithms- Partitioning based placement algorithms-cluster growthQuadratic assignment-resistive network optimization.

UNIT IV – ROUTING and COMPACTION

Global Routing- Detailed routing- Over the cell routing and via minimization-clock and power routing. Problem Formulation - Classification of Compaction algorithms- 3/2 dimensional compaction-2D compaction- Hierarchical compaction- Recent trends in Compaction.

UNIT V - ISSUES ON INTERCONNECTS

Timing driven Interconnect synthesis-Buffer insertion basics-Generalised buffer insertion-Buffering in layout environment-Global interconnect planning. Introduction to physical design for 3D circuits.

TEXTBOOKS:

1. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwar Academic Publishers, 2002.
2. S.H. Gerez, “Algorithms for VLSI Design Automation”,John Wiley & Sons, 2008.

REFERENCES:

1. Sung Kyu Lim, “Practice Problems in VLSI physical design Automation”,Springer, 2008.

2. charles J . Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar ,"Hand book of algorithms of Physical design Automation ",CRC press, 2009.
3. Jeffrey D Ullman"Computational aspects of VLSI",Computer Science Press, 1984.
4. Sadiq M .Sait, Habib Youssef,"VLSI Physical design automation theory and Practice",World Scientific Publishing,1999.

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CMOS ANALOG IC DESIGN

UNIT-1

MOS Devices and ModelingThe MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT –2

Analog CMOS Sub-Circuits MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT –3

CMOS Amplifiers Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT –4

CMOS Operational Amplifiers Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAMP.

UNIT –5

Comparators Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXTBOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, PaulJ. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCES:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition. 3.

CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

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CPLD AND FPGA ARCHITECURES AND APPLICATIONS

UNIT-1

Introduction to Programmable Logic Devices Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-2

Field Programmable Gate Arrays Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT –3

SRAM Programmable FPGAs Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT –4

Anti-Fuse Programmed FPGAs Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT –5

Design Applications General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXTBOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCES:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/ Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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CMOS DIGITAL IC DESIGN

UNIT-1

MOS Design Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III

Sequential MOS Logic Circuits Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT-IV

Dynamic Logic Circuits Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V

Semiconductor MemoriesTypes, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXTBOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011. 2.

CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCES:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

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I Year – I SEMESTER

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ASIC DESIGN
(ELECTIVE-I)

UNIT I

Introduction to ASIC'S - Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort -Library cell design - Library architecture .

UNIT II

Programmable ASIC'S - Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III

Programmable ASIC logic cells - 25 Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX -Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV

ASIC floor planning placement and routing - ASIC Construction: Physical Design- System Partitioning- FPGA Partitioning- Partitioning Methods. Floorplanning and Placement: Floorplanning- Placement- Physical Design Flow. Routing: Global Routing - Detailed Routing- Special Routing. Design checks

UNIT V

Optimization algorithms - Planar subset problem(PSP) -single layer global routing single layer detailed routing wire length and bend minimization technique-over the cell(OTC) Routing-multichip modules(MCM)-Programmable logic arrays-Transistor chaining-Weinberger Arrays-Gate Matrix Layout-1D compaction-2D compaction

TEXTBOOKS:

1. M. J. S. Smith, "Application Specific Integrated Circuits",Addison -Wesley Longman Inc., 1997.

REFERENCES:

1. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach",Prentice Hall PTR, 2003.

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ADVANCED OPERATING SYSTEMS
(ELECTIVE I)

UNIT-I

Introduction to Operating Systems, Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT-II

Introduction to UNIX and LINUX Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT –III

System Calls:System calls and related file structures, Input / Output, Process creation & termination. Inter Process Communication:Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV

Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues. Communication in Distributed Systems:Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V

Synchronization in Distributed Systems:Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions Deadlocks:Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXTBOOKS :

1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.

2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.

3. The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCES:

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.

2. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.

3. Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley

4. UNIX User Guide – Ritchie & Yates.

5. UNIX Network Programming - W.Richard Stevens, 1998, PHI

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SOFT COMPUTING TECHNIQUES
(ELECTIVE I)

UNIT –I

Introduction: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II

Artificial Neural Networks: Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III

Fuzzy Logic System: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV

Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and anD-colony search techniques for solving optimization problems.

UNIT –V

Applications: GA application to power system optimization problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXTBOOKS:

1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999. 2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCES:

1. Fuzzy Sets, Uncertainty and Information - Klir G.J. & Folger T.A., Prentice-Hall of India Pvt. Ltd., 1993.

2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994. 3. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.

4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi. 5. Elements of Artificial Neural Networks - Kishan Mehrotra, Chelkuri . Mohan, Sanjay Ranka, Penram International.

6. Artificial Neural Network –Simon Haykin, 2nd Ed., Pearson Education.

7. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.

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I Year – I SEMESTER

L	P	C
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DIGITAL DESIGN USING HDL
(ELECTIVE II)

Unit 1:

Digital Logic Design using VHDL Introduction, designing with VHDL, design entry methods, logic synthesis , entities , architecture , packages and configurations, types of models: dataflow , behavioral , structural, signals vs. variables, generics, data types, concurrent vs. sequential statements , loops and program controls.

Digital Logic Design using Verilog HDL Introduction, Verilog Data types and Operators, Binary data manipulation, Combinational and Sequential logic design, Structural Models of Combinational Logic, Logic Simulation, Design Verification and Test Methodology, Propagation Delay, Truth Table models using Verilog.

Unit 2:

Combinational Logic Circuit Design using VHDL Combinational circuits building blocks: Multiplexers, Decoders , Encoders , Code converters, Arithmetic comparison circuits , VHDL for combinational circuits , Adders-Half Adder, Full Adder, Ripple-Carry Adder, Carry Look-Ahead Adder, Subtraction, Multiplication.

Sequential Logic Circuit Design using VHDL Flip-flops, registers & counters, synchronous sequential circuits: Basic design steps, Mealy State model, Design of FSM using CAD tools, Serial Adder Example, State Minimization, Design of Counter using sequential Circuit approach.

Unit 3:

Digital Logic Circuit Design Examples using Verilog HDLBehavioral modeling , Data types, Boolean-Equation-Based behavioral models of combinational logics , Propagation delay and continuous assignments, latches and level-sensitive circuits in Verilog, Cyclic behavioral models of flip-flops and latches and Edge detection, comparison of styles for behavioral model; Behavioral model, Multiplexers, Encoders and Decoders, Counters, Shift Registers, Register files, Dataflow models of a linear feedback shift register, Machines with multi cycle operations, ASM and ASMD charts for behavioral modeling, Design examples, Keypad scanner and encoder.

Unit 4:

Synthesis of Digital Logic Circuit Design Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic with latches and flip-flops, Synthesis of Explicit and Implicit State Machines, Registers and counters.

Unit 5:

Testing of Digital Logic Circuits and CAD Tools Testing of logic circuits, fault model, complexity of a test set, path-sensitization, circuits with tree structure, random tests, testing of

sequential circuits, built in self test, printed circuit boards, computer aided design tools, synthesis, physical design.

TEXTBOOKS:

1. Stephen Brown & Zvonko Vranesic, “Fundamentals of Digital logic design with VHDL”, Tata McGraw Hill,2nd edition.
2. Michael D. Ciletti, “Advanced digital design with the Verilog HDL”, Eastern economy edition, PHI.

REFERENCES:

1. Stephen Brown & Zvonko Vranesic, “Fundamentals of Digital logic with Verilog design”, Tata McGraw Hill,2nd edition.
2. Bhaskar, “VHDL Primer”,3rd Edition, PHI Publications.
3. Ian Grout, “Digital systems design with FPGAs and CPLDs”, Elsevier Publications.

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ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE II)

UNIT-I

Fundamentals of Computer Design Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl‟slaw. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, Operations in the instruction set.

UNIT-II

PipelinesIntroduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy DesignIntroduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory. **UNIT-III**

Instruction Level Parallelism (ILP)-The Hardware Approach Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo‟s approach, Branch prediction, High performance instruction delivery- Hardware based speculation. ILP Software ApproachBasic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT-IV

Multi Processors and Thread Level Parallelism Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT-V

Inter Connection and Networks Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXTBOOKS:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCES:

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.
3. Advanced Computer Architecture - A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk, Pearson Ed.

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HARDWARE SOFTWARE CO-DESIGN
(ELECTIVE II)

UNIT-I

Co- Design IssuesCo- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT-II

Prototyping and Emulation Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure Target ArchitecturesArchitecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III

Compilation Techniques and Tools for Embedded Processor Architectures Modern embedded architectures, embedded software development needs, compilation Technologies, practical consideration in a compiler development environment.

UNIT-IV:

Design Specification and Verification Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT-V:

Languages for System-Level Specification and Design-I System-level specification, design representation for system level synthesis, system level specification languages. Languages for

System-Level Specification and Design-II Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXTBOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, MariagiovannaSami, 2002, Kluwer Academic Publishers.

REFERENCES:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R.Schaumont - 2010 – Springer Publications.

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VLSI LABORATORY-I

The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/ Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/ FPGA kits).

- The students are required to acquire the knowledge in both the Platforms (Xilinx and Mentor graphics) by perform at least FIVE experiments on each Platform.

List of Experiments:

1. Realization of Logic gates. 2. Parity Encoder.
3. Random Counter
4. Single Port Synchronous RAM. 5. Synchronous FIFO.
6. ALU.
7. UART Model.
8. Dual Port Asynchronous RAM.
9. Fire Detection and Control System using Combinational Logic circuits. 10. Traffic Light Controller using Sequential Logic circuits
11. Pattern Detection using Moore Machine.
12. Finite State Machine(FSM) based logic circuit.

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mento Graphics-Precision RTL

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

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I Year – II SEMESTER	**L**	**P**	**C**
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LOW POWER VLSI DESIGN

UNIT-I

Fundamentals of Low Power VLSI Design Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT-II

Low-Power Design Approaches Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT-III

Low-Voltage Low-Power Adders Introduction, Standard Adder Cells, CMOS Adder‟s Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT-IV

Low-Voltage Low-Power Multipliers Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT-V

Low-Voltage Low-Power Memories Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXTBOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.

2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCES:

1. Low Power CMOS Design – Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
2. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
3. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
4. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.

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I Year – II SEMESTER	**L**	**P**	**C**
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CMOS MIXED SIGNAL CIRCUIT DESIGN

UNIT-I

Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-II

Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III

Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time interleaved converters.

UNIT-V

Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXTBOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002 2.
CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCES :

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog convertersRudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

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RECONFIGURABLE ARCHITECTURES FOR VLSI

UNIT I - RECONFIGURABLE COMPUTING HARDWARE

Logic- computational fabric, Array and interconnect-Extended logic- Configuration- Reconfigurable processing fabric architectures-RPF integration into traditional computing systems- operating system support for reconfigurable computing- Evolvable FPGA 16

UNIT II - MAPPING DESIGNS INTO RECONFIGURABLE PLATFORMS

Structural mapping- integrated mapping- mapping for heterogeneous resources-Placement problem – clustering- simulated annealing – partition based placement – analytical placement- partitioning for granularity- partitioning of parallel programs- instance specific design

UNIT III - COMPUTATIONAL ARCHITECTURES FOR FP

Precision analysis for fixed point computation- Distributed arithmetic for FPGA – CORDIC architectures for FPGA- Boolean satisfiability – SAT solvers

UNIT IV - OPTICAL RECONFIGURATION MODELS

Simulation and scalability- Models, Basic algorithmic techniques- optical models – complexities of optical models- run time reconfigurability- Design and implementation

UNIT V - MULTI CORE ARCHITECTURES

Multi core and many core architectures-state of theart multi core operating systems-parallelism and performance analysis

TEXTBOOKS:

1. Scott Hauck, André Dehon ,“Reconfigurable computing: the theory and practice of FPGA-based computation”, Morgan Kaufmann publishers, 2008.

2. Ramachandran Vaidhyanathan and Jerry. L. Trahan “Dynamic Reconfiguration: Architectures and Algorithms”, Kluwer Academic publishers, 2003.

REFERENCES:

1. Andras Vajda, “Programming many core chips”,Springer, 2011

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DESIGN FOR TESTABILITY

UNIT-I

Introduction to Testing Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II

Logic and Fault Simulation Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for Truevalue Simulation, Algorithms for Fault Simulation.

UNIT –III

Testability Measures SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV

Built-In Self-Test The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V

Boundary Scan Standard Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXTBOOKS:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers-2005

REFERENCES:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House-1990.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press-1997.

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SCRIPTING LANGUAGES
(ELECTIVE-III)

UNIT-I

Introduction to Scripts and Scripting Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT-II

Advanced PERL Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT-III

TCL The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/ output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT-IV

Advanced TCL The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications „Internet-aware“, „Nuts-and-bolts“ internet programming, Security issues, running untrusted code, The C interface.

UNIT-V

TK, JavaScript and OOP Concepts Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXTBOOKS:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

REFERENCES: :

1. Tcl/Tk: A Developer‟s Guide- Clif Flynt, 2003, Morgan Kaufmann SerieS. 2.

Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition.

3. Tcl 8.5 Network Programming book- Wojciech Kocjan and Piotr Beltowski, Packt Publishing.
4. Tcl/Tk 8.5 Programming Cookbook- Bert Wheeler

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DIGITAL SIGNAL PROCESSORS & ARCHITECTURS
(ELECTIVE III)

UNIT-I

Introduction to Digital Signal Processing Introduction, a Digital signal processing system, the sampling process, discrete time sequences.

Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation. Computational Accuracy in DSP Implementations Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II

Architectures for Programmable DSP Devices Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT-III

Programmable Digital Signal Processors Commercial Digital signal processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-IV

Analog Devices Family of DSP Devices Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-

2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control

Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT-V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXTBOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCES:

1. Digital Signal Processors, Architecture, Programming and ApplicationsB. Venkataramani and M. Bhaskar, 2002, TMH.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
3. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
4. The Scientist and Engineer‟s Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997

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VLSI SIGNAL PROCESSING
(ELECTIVE-III)

UNIT-I

Introduction to DSPTypical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT-II

Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multi rate systems Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT-III

Systolic Architecture Design Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays **UNIT-IV**

Fast Convolution Introduction – Cook-Toom Algorithm – Wino gard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT-V

Low Power Design Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

TEXTBOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.

2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCES:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice
Hall.

2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

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HIGH SPEED VLSI
(ELECTIVE – IV)

UNIT I - CLOCKED LOGIC STYLES

Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked pass Gate Logic Non Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked pass Gate Families.

UNIT II - CIRCUIT DESIGN MARGINING AND DESIGN VARIABILITY

Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise.

UNIT III - LATCHING STRATEGIES

Latching Strategies, Basic Latch Design, Latching Differential Logic, Race Free Latches for Pre-charged Logic, Asynchronous Latch Techniques.

UNIT IV - INTERFACE TECHNIQUES

Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection, Skew Tolerant Design

UNIT V - CLOCKING STYLES

Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

TEXTBOOKS:

1. Kerry Bernstein, Keith M. Carrig, “High Speed CMOS Design Styles”, Kluwer Academic Publishers, 2002.

2. Evan Sutherland, Bob Stroll, David Harris,” Logical Efforts, Designing Fast CMOS Circuits”,Kluwer Academic Publishers, 1999

REFERENCES :

1. David Harris, “Skew Tolerant Domino Design”,IEEE Journal of Solid State Circuits, 2001..

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OPTIMIZATION TECHNIQUES IN VLSI DESIGN
(ELECTIVE IV)

UNIT-I

Statistical ModelingModeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom‟s model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT-II

Statistical Performance, Power and Yield Analysis Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, Highlevel statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT-III

Convex Optimization Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Polynomial fitting.

UNIT-IV

Genetic Algorithm Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation-Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placementGASP algorithm-unified algorithm.

UNIT-V

GA Routing Procedures and Power Estimation Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GAStandard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

TEXTBOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power -Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation -Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.

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REFERENCES :

1. Convex Optimization Stephen Boyd, Lieven Vandenberghe, Cambridge University Press,2004.

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SEMICONDUCTOR MEMORY DESIGN AND TESTING
(ELECTIVE IV)

UNIT-I

Random Access Memory Technologies SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II

Non-volatile Memories Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT-III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT-IV

Semiconductor Memory Reliability and Radiation Effects General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues,

Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT-V

Advanced Memory Technologies and High-density Memory Packing TechnologiesFerroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

TEXTBOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.

REFERENCES:

1. Modern Semiconductor Devices for Integrated Circuits − Chenming CHu, 1st Ed., Prentice Hall.

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VLSI LABORATORY-II

PART-A: VLSI Lab (Back-end Environment)

- The students are required to design and implement the Layout of the following Experiments of any SIX using CMOS 130nm Technology with Mentor Graphics Tool.

List of Experiments:

1. Inverter Characteristics. 2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter. 5. Static RAM Cell.
6. Dynamic RAM Cell. 7. ROM
8. Digital-to-Analog-Converter. 9. Analog-to-Digital Converter.

PART-B: Mixed Signal Simulation

- The students are required to perform the following experimental concepts with suitable complexity mixed-signal application based circuits of any FOUR (circuits consisting of both analog and digital parts) using necessary software tools.

List of experimental Concepts:

Analog circuit simulation.

Digital circuit simulation.

Mixed signal simulation.

Layout Extraction.

- Parasitic values estimation from layout.

Layout Vs Schematic.

- Net List Extraction.
- Design Rule Checks.

Lab Requirements: Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool, Mixed Signal simulator

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.